Matira3 Title Page/Index

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034	DDR4 DIMM8 CPU0.CHC.D1	
035	DDR4 DIMM2 CPU0.CHD.D0	
036	DDR4 DIMM6 CPU0.CHD.D1	
037	EMPTY	
038	EMPTY	
039	EMPTY	
040	EMPTY	
041	EMPTY	N/A
042	EMPTY	
043	EMPTY	
044	EMPTY	

P.	Contents	Function
045	EMPTY	N/A
046	EMPTY	
047	EMPTY	
048	EMPTY	
049	EMPTY	
050	EMPTY	
051	EMPTY	N/A
052	EMPTY	
053	EMPTY	
054	EMPTY	
055	EMPTY	
056	EMPTY	
057	EMPTY	
058	EMPTY	
059	EMPTY	
060	EMPTY	
061	EMPTY	
062	EMPTY	
063	DMI_LAI/UPLINK	DEBUG
064	CPU Common Logic - 1OF2	LOGIC
065	CPU Common Logic - 2OF2	
066	Clock Buffer /TCM	CLOCK/TCM
067	EMPTY	
068	PCIE G3 X16 - Slot1_CPU0_8x	PCIE SLOT
069	PCIE G3 X16 - Slot2_CPU0	
070	PCIE G3 X16 - Slot4_CPU0	
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075	PCIE Storage Connector	STORAGE
076	PCH CLOCK/HDA/JTAG	PCH
077	PCH USB/PCIE/DMI	
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083	STRAP	LOGIC
084	Miscellaneous	
085	EC Embedded Controller	EC
086	EMPTY	
087	CPLD - 1OF2	CPLD
088	CPLD - 2OF2	

P.	Contents	Function
089	GBE I219 Jacksonville	LAN
090	EMPTY	
091	EMPTY	
092	Audio Codec	AUDIO
093	Audio Connector	
094	USB 3.0 Connector - 1OF3	USB
095	USB 3.0 Connector - 2OF3	
096	FRONT USB 3.0(F_TypeA&SD)	
097	INT USB 2.0	
098	FRONT USB 3.0(F_TypeC)	
099	USB 3.0 Connector - 3OF3	
100	EMPTY	
101	EMPTY	
102	SATA Connector	STORAGE
103	PS/2 KBMS/Serial	PS/2
104	Power Conn/Front Panel	CONN
105	Thermal Sensor	SENSOR
106	Fan Connector	FAN
107	TPM/SPI	TPM/SPI
108	Debug/Label/Misc	XDP
109	MERGED XDP - DCI	DCI
110	SMBUS MUX	SMBUS
111	OTHER	OTHER
112	VR, CPU0 CORE _PWM(IFX)	CPU0 VR
113	VR, CPU0 CORE OUTPUT	
114	VR, CPU0_VCCSA OUTPUT	
115	VR, CPU0_VCCIO CONTROLLER	
116	VR, CPU0_VCCIO_PHASE	
117	EMPTY	
118	EMPTY	
119	EMPTY	
120	EMPTY	N/A
121	EMPTY	
122	EMPTY	
123	EMPTY	
124	EMPTY	
125	EMPTY	
126	EMPTY	
127	EMPTY	
128	VR, CPU0_VDDQ012_PWM(Ti)	CPU0 MEM VR
129	VR, CPU0_VDDQ012_OUT	
130	VR, CPU0_VDDQ345_PWM(TI)	
131	VR, CPU0_VDDQ345_OUT	
132	EMPTY	

P.	Contents	Function
133	EMPTY	N/A
134	EMPTY	
135	EMPTY	
136	VR, CPU0 MEMORY VPP	MEM VTT
137	EMPTY	PCH VR
138	VR, MEMORY VTT (TI)	
139	VR, +12VAUX_PCH	SYS VR
140	VR, +1V0/+1V8_AUX	
141	VR, +5V/+3_3V(Dell)	
142	VR+5/+3.3V_STB&+3.3V_SLOT	LOM VR
143	LOADSWITCH, +5V/+3V	
144	EMPTY	N/A
145	PGPPA_AUX_PCH	PCH VR
146	Changelist A	
147	Changelist B	

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COMPRESSED IMAGE

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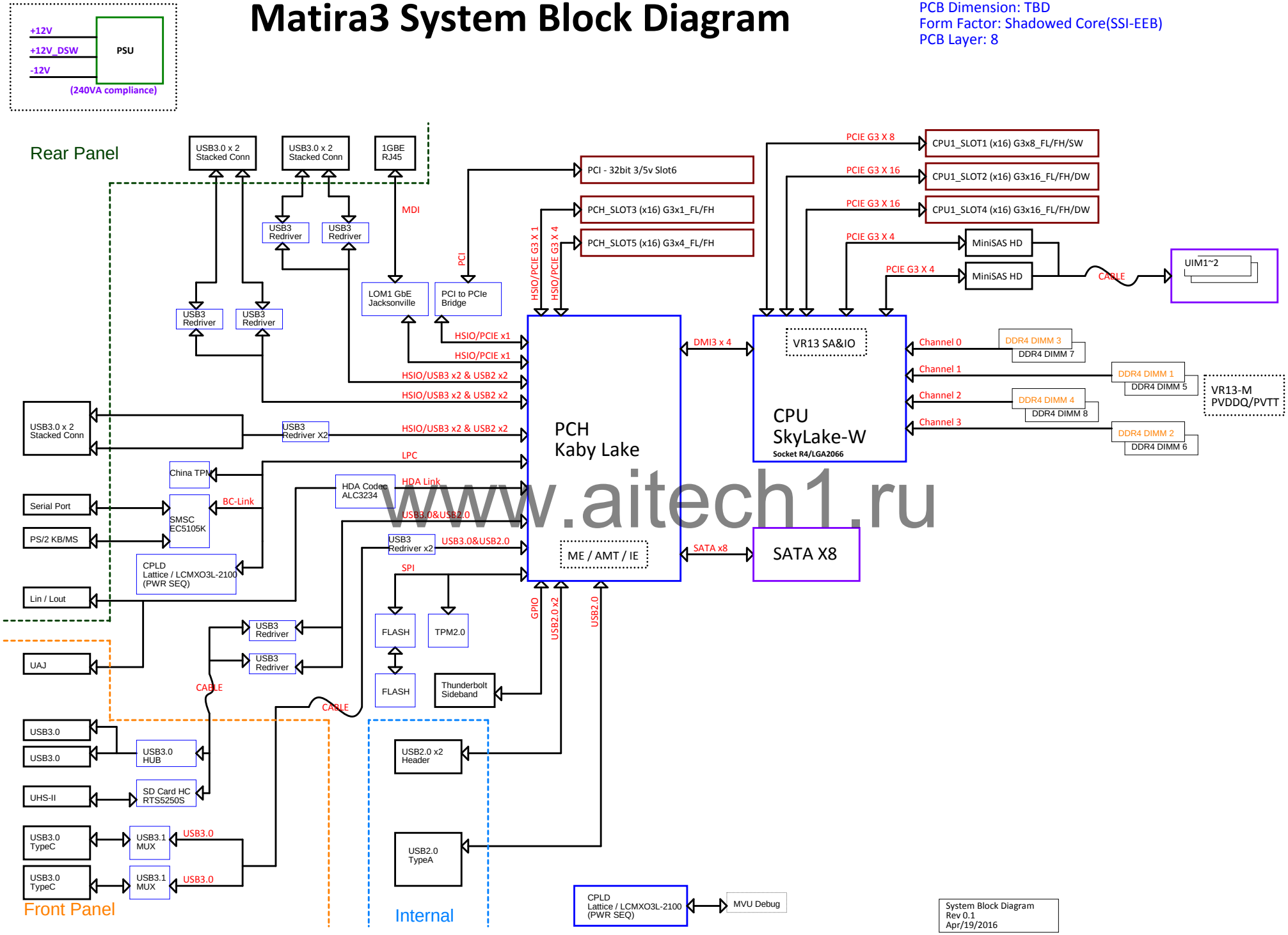
Matira3 System Block Diagram

PCB Dimension: TBD
Form Factor: Shadowed Core(SSI-EEB)
PCB Layer: 8



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System Block Diagram
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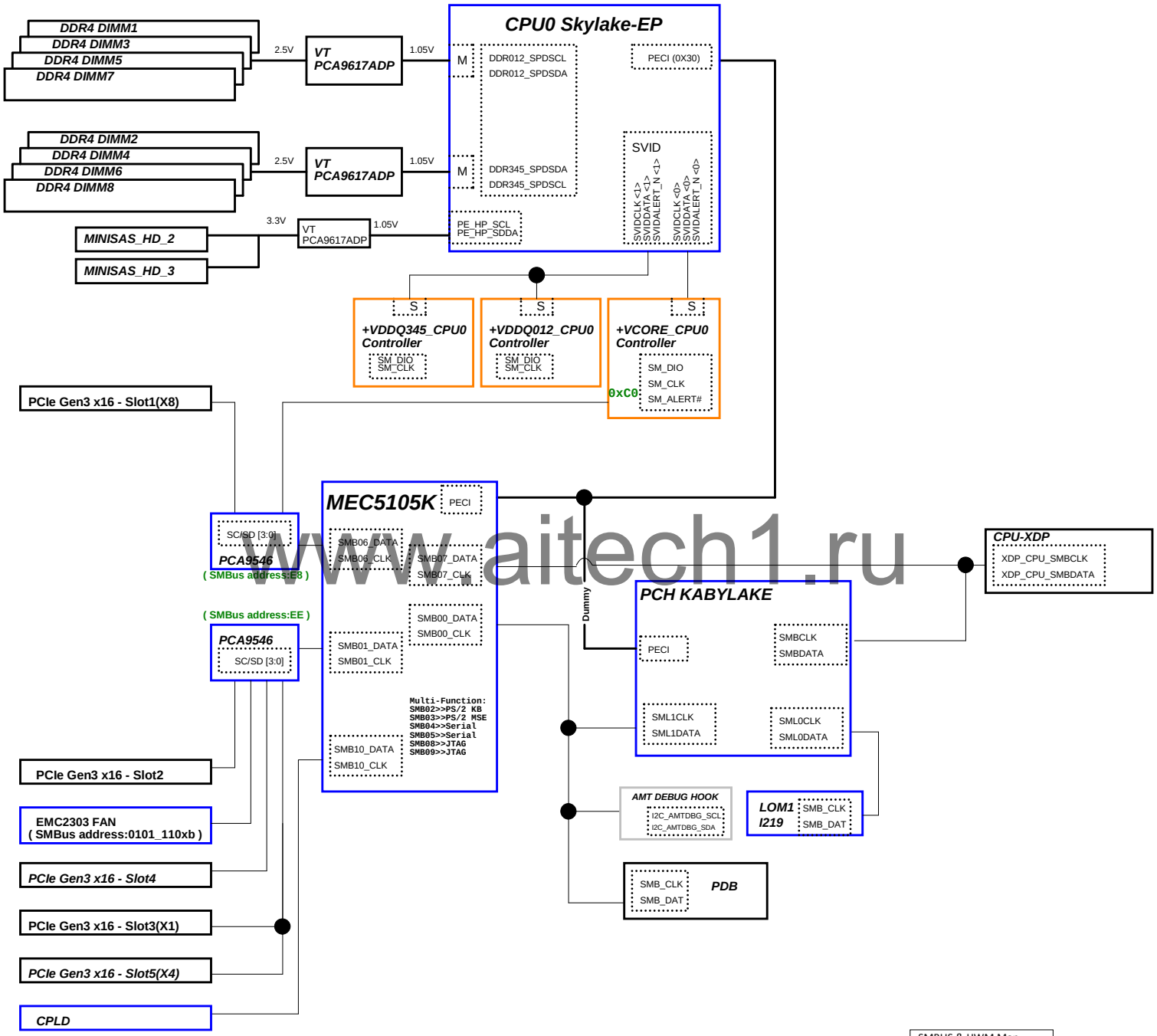
Matira 3 SMBUS & HWM Diagram



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SMBUS & HWM Map
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Apr/19/2016

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TITLE	I2C/SMBUS and HWM Map		
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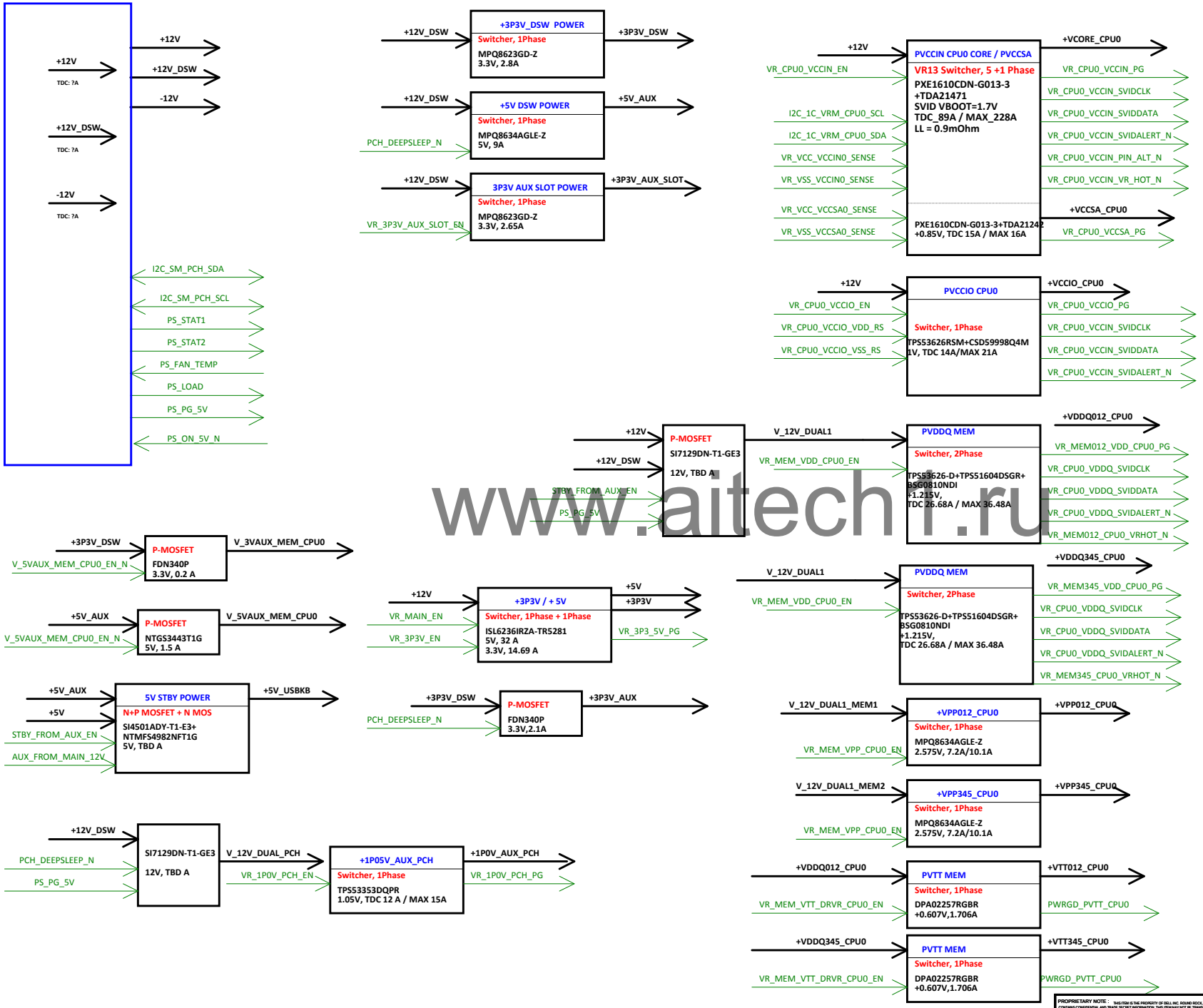
COMPRESSED IMAGE

Matira 3 Power Delivery Diagram



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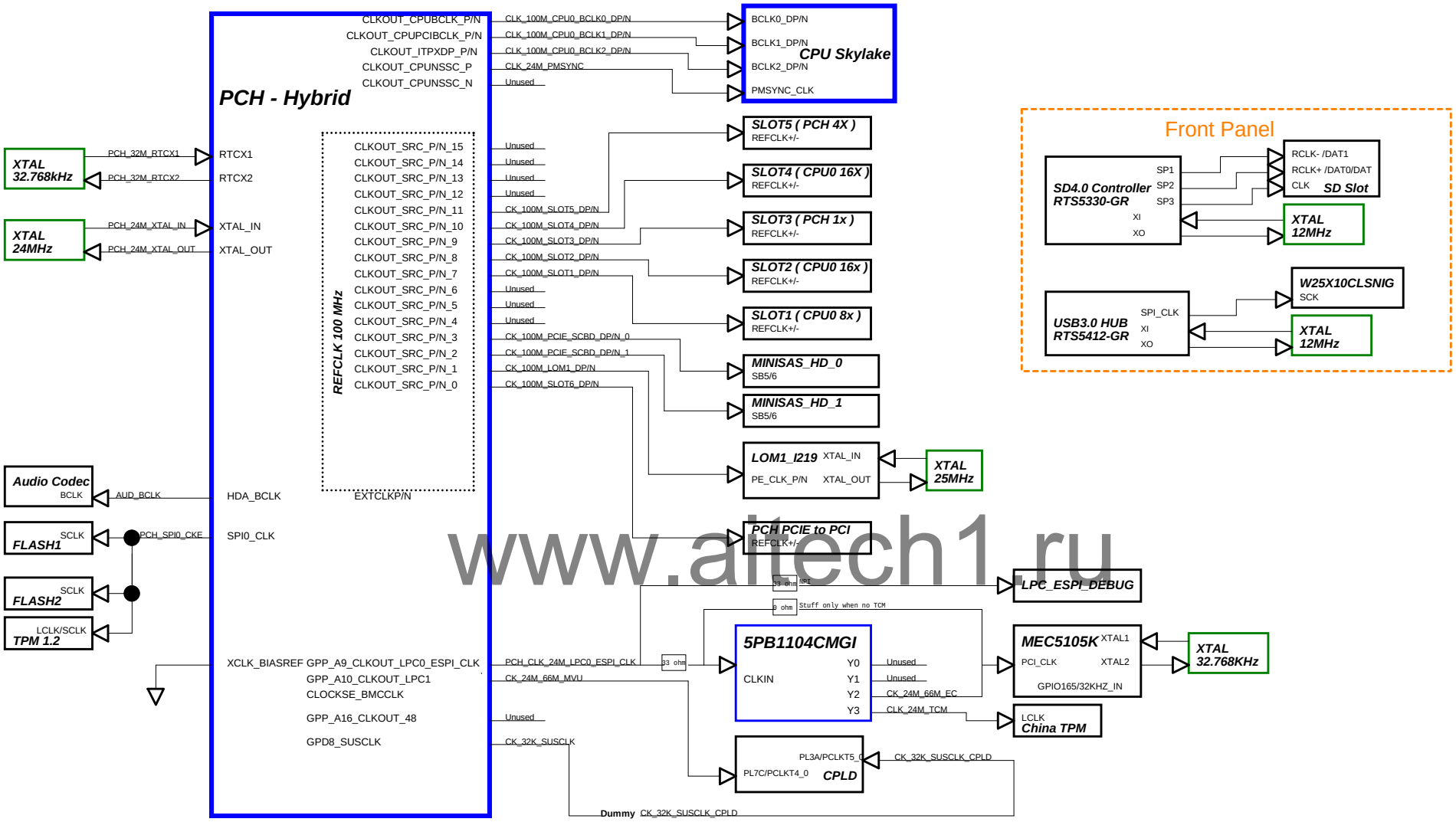
COMPRESSED IMAGE

Matira3 Clock Distribution Diagram

PCH Hybrid Clock Mode



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Clock Distribution Diagram
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Matira3 Power Sequence Diagram

G3 to S5 / S5 to S0 Timing Diagram

Source	Destination	Signal_Name	
Board	PCH	V_3V_VBAT	
Board	PCH	PCH_RTCRST_N	[>9ms] VccRTC stable to RTEST# High.
PSU	Board	+12V_DSW	[<1.5s] AC Applied to +12V_DSW to Stable.
Board	PCH	+5V_DSW / +3P3V_DSW	[>9ms] VccRTC Stable to start of VccDSW voltage ramp.
Board	PCH	VR_PCH_DSW_PWROK	[>9us] RTCRST# to DPWROK High. / [>10ms] +3P3V_DSW stable to DPWROK High.
Board	PCH	PCH_32M_RTCX[2:1]	[>95ms] DPWROK to RTCCLK to Stable.
PCH	CPLD / EC / VR	PCH_DEEPSLEEP_N	[>95ms] DPWROK to SLP_SUS# deassertion.
VR	VR	V_12V_DUALx_MEMx	[>4ms] RC Delay from SLP_SUS#
VR	Board	+5V_AUX	
VR	Board	+3P3VAUX	
CPLD / EC	VR	VR_3P3V_AUX_SLOT_EN	
VR	Board	+3P3V_AUX_SLOT	
CPLD / EC	VR	VR_1P0V_PCH_EN	
VR	Board	+1P0V_AUX_PCH	
VR	Board	VR_1P0V_PCH_PG	
CPLD	PCH	PCH_RSMRST_N	[>10ms] Vcc_prim stable to RSMRST# high. (CPLD delay 11ms)
PCH	CPLD	CK_32K_SUSCLK	[>5ms] SLP_SUS# to SUSCLK to Stable. / [>5ms] RSMRST# to SUSCLK to Stable.
PCH	Board (CPLD / EC)	PCH_SUSWARN_N	
Board	PCH	PCH_SUSACK_N	[>200ms] SUSWARN# to SUSACK# to High.
PCH	Board	PCH_WAKE_N	WAKE
Board	PCH / CPLD / EC	PCH_PWRBTN_N	
PCH	Board / CPLD / EC	PCH_SLP_S[5,4,3]_N	[>30us] SLP_S5# high to SLP_S4# high / [>30us] SLP_S4# high to SLP_S3# high
PCH	Board / CPLD / EC	PCH_SLP_A_N	
PCH	VR	PCH_SLP_LAN_N	WOL
VR	LOM1	+3P3V_DSW_LAN	[<20ms] SLP_LAN# (or LANPHYPC) rising to VccLANPHY High and Stable.
CPLD / EC	PSU	PS_ON	
PSU	Board	+12V	
PSU	Board / CPLD / EC	PS_PG_3P3_N	[100ms-400ms] P12V to PWRGD_PS_PWROK to High.
CPLD / EC	VR	VR_MAIN_EN (VR_3P3V_EN)	
VR	Board	+5V	
VR	Board	+3P3V	
VR	CPLD	VR_3P3_5V_PG	PCH power rails switchs from aux with the main rail bring-up after SLP_S3# high.
CPLD / EC	Board	AUX_FROM_MAIN_N	
CPLD / EC	Board	STBY_FROM_AUX_EN	Only exit in S3
VR	Board	+5V_USBKB	
VR	PCH	+3P3VAUX	
VR	PCH	+1P0V_AUX_PCH	
CPLD / EC	VR	VR_MEM_VPP_CPU0_EN	(CPLD delay 12ms)
VR	DRAM / CPU	+VPP[012,345]_CPU0	Vboot = 2.5V. Switch VPP from standby based on SLP_S4 and PS_PWROK
CPLD / EC	VR	VR_MEM_VDD_CPU0_EN	
VR	DRAM / CPU	+VDDQ[012,345]_CPU0	[>0s] VPP_2P5V High to VDDxx High. Vboot = 1.2V
VR	EC / CPLD	VR_MEM[5:0]_VDD_CPU0_PG	
CPLD / EC	VR	VR_MEM_VTT_DRVR_CPU0_EN	
VR	DRAM	+VTT[012,345]_CPU0	[>0s] VDDxx High to VTT High.
CPLD / EC	Board	CPU_MEM_VDD_PG	[>0s] VDDxx High to DRAMPWRGD High.
CPLD	CPU	PWRGD_CPU0_[M:A]_DRAM_GTL	
CPLD / EC	VR	VR_CPU0_VCCIO_EN	
VR	CPU	+VCCIO_CPU0	[>0s] VDDxx High to VCCIO High. Vboot = 1.0V
VR	CPLD / EC	VR_CPU0_VCCIO_PG	
CPLD / EC	VR	VR_CPU0_VCCIN_EN	
VR	CPU	+VCORE_CPU0	[>0s] VCCIO High to VCCIN High. Vboot = 1.7V
VR	CPLD / EC	VR_CPU0_VCCIN_PG	
VR	CPU	+VCCSA_CPU0	[>0s] VCCIN High to VCCSA High. Vboot = 0.9V
VR	CPLD / EC	VR_CPU0_VCCSA_PG	

Source	Destination	Signal_Name	
CPLD / EC	PCH	PCH_PWROK_PG	[>99ms] Vcc_main (VR_3P3_5V_PG) stable to PCH_PWROK
PCH	Board	PCH isClocks	[10ms] INT_CLK_EN assertion releases PCH Clocks externally.
PCH	CPLD / EC	PCH_PROC_PWRGD	
CPLD / EC	CPU	CPLD_PROC_PWRGD	Set to 5ms for DBxx stabilization in Hybrid mode. (100ms default)
CPLD / EC	PCH	PCH_SYS_PWROK	
PCH	CPLD / EC	PCH_PLTRST_N	[t1001(10ms)+ 60us] CPUPWRGD to RST_PLTRST_N to High.
CPLD / EC	Board	RST_PCIE_PCH_PERST_N	
CPU	CPLD / EC	H_CPU0_FIVR_FAULT_GTL	
CPU	DRAM	M_xxx_RESET_N	Under BIOS Control

S0 to S5 Timing Diagram

- To Be Updated -

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Power Sequence Diagram
Rev 0.1
Aug/15/2016

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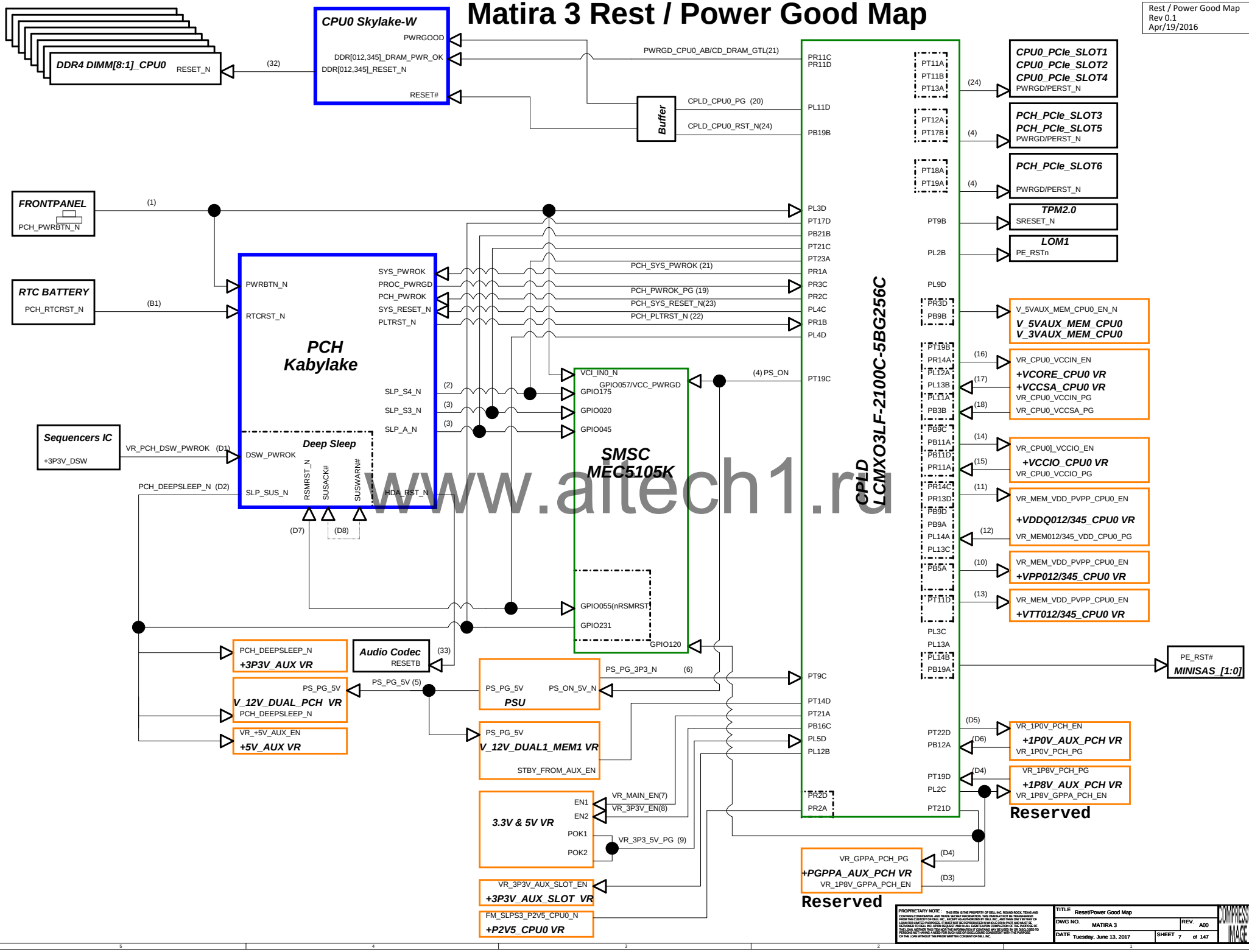
J-COMPRESSED IMAGE

Matira 3 Rest / Power Good Map

Rest / Power Good Map
Rev 0.1
Apr/19/2016



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TITLE	Reset/Power Good Map
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Matira 3 Strap/IRQ/IDSel Table

PCH Functional Strap

COMPRESSED IMAGE

COMPRESSED IMAGE

COMPRESSED IMAGE

COMPRESSED IMAGE

PCH IRQ

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CPU Functional Strap

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Strap/IRQ/IDSel Table
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Apr/19/2016

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TITLE:	Strap/IRQ/IDSel Table		
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Matira 3 GPIO Table (1 of 2)

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Matira 3 GPIO Table (2 of 2)

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Matira 3 XDP Block Diagram

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TITLE:	MERGED XDP - Block Diagram		
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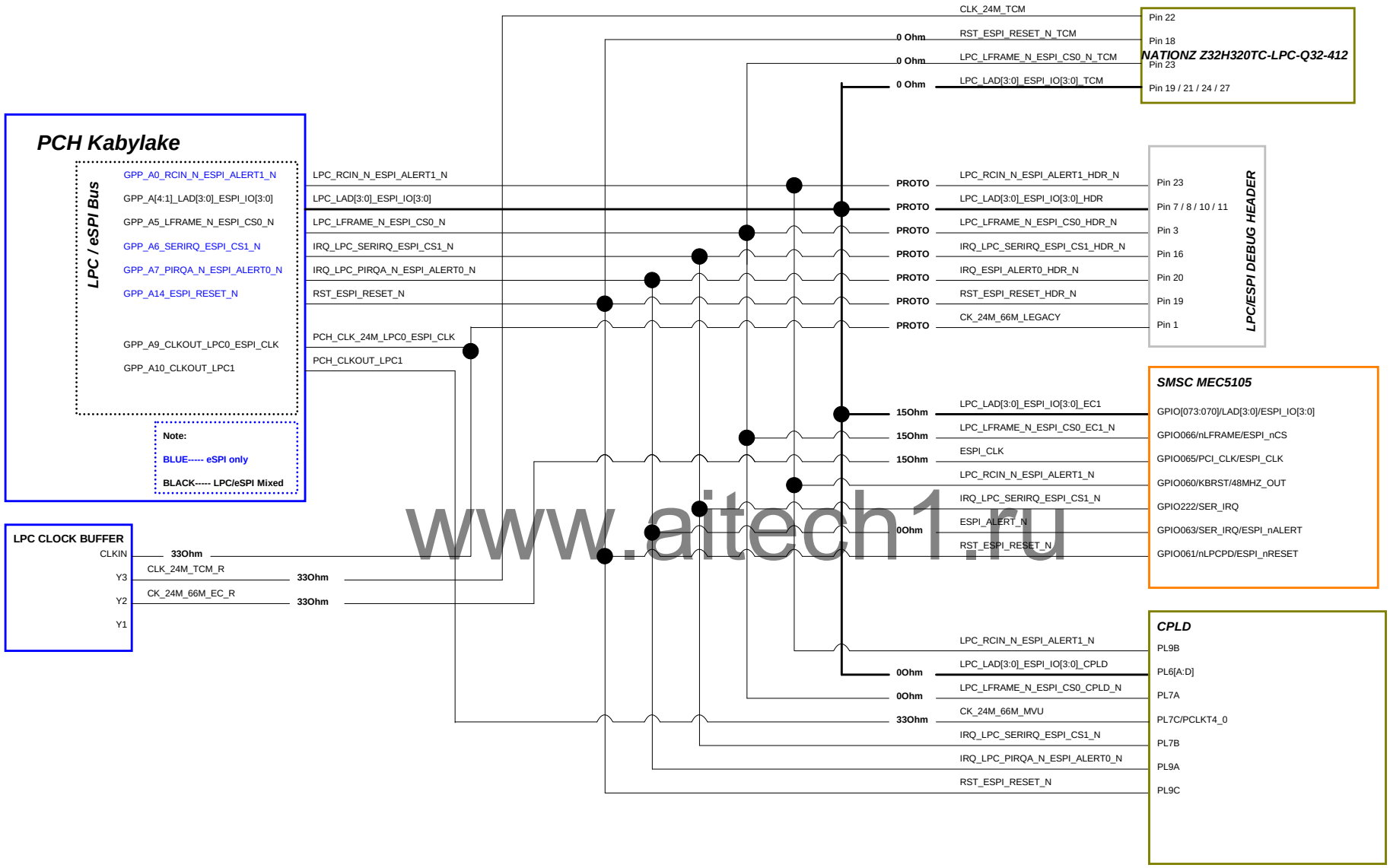
Matira 3 LPC/eSPI Block Diagram



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LPC/eSPI Block Diagram
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TITLE	Matira 7 LPC/eSPI Block Diagram		
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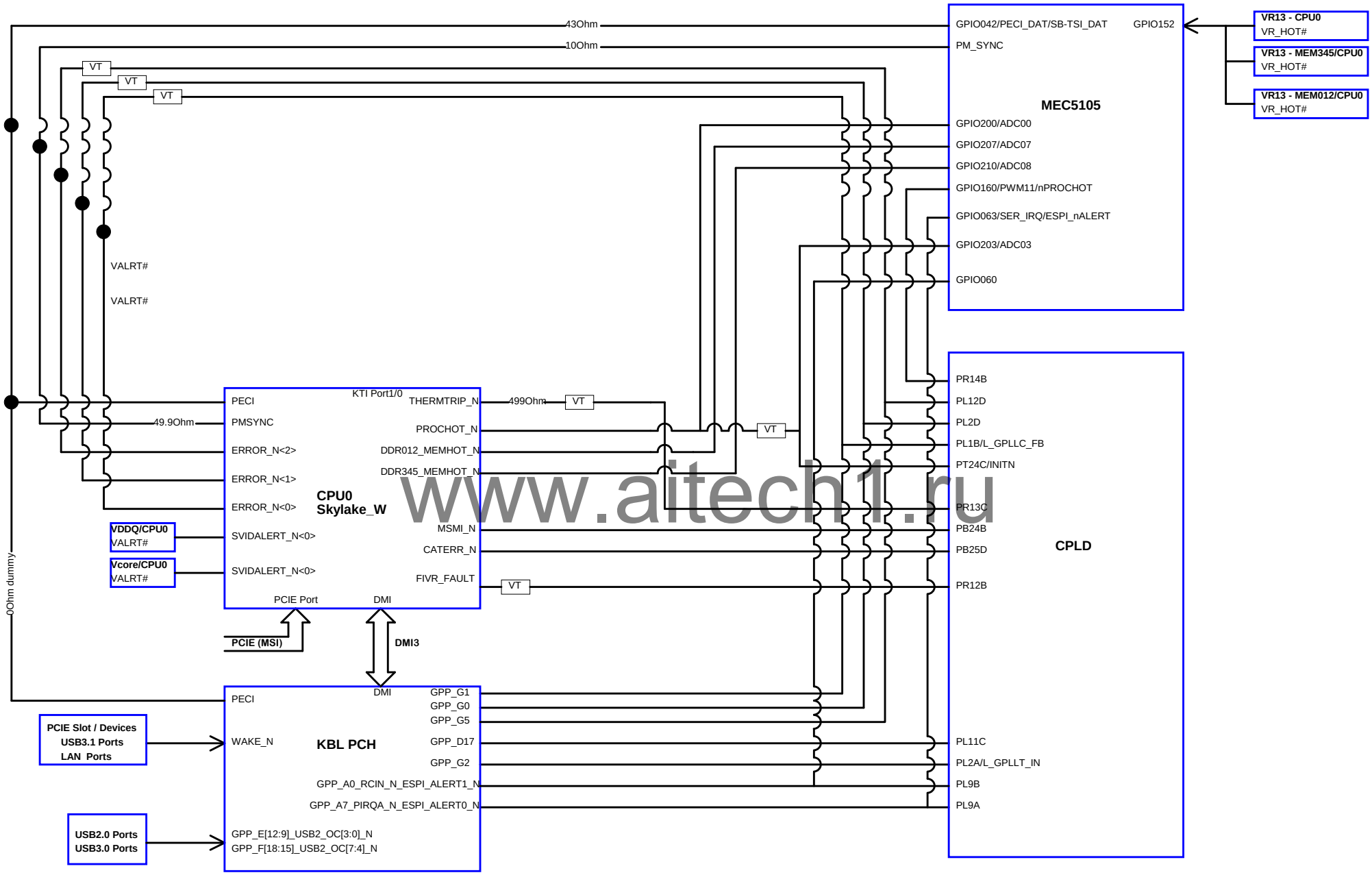
UNCLASSIFIED IMAGE

Matira 3 Error Management Block Diagram

Error Management Block Diagram
Rev 0.1
Apr/19/2016



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TITLE	Error Management Diagram		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	13 of 147

COMPRESSED IMAGE

Matira 3 System Power Rail

				M3		Moff				
No.	**Power Rails**	**Voltage**	**S0**	**S3**	**S4/S5**		**DSW**	**G3**	**Source**	**Control Signal**
1	V_3V_VBAT	3V	ON	ON	ON	ON	ON	ON	RTC Battery	RTC Battery
2	+12V_DSW	12V	ON	ON	ON	ON	ON	OFF	PSU	Adaptor in
3	+3P3V_DSW	3.3V	ON	ON	ON	ON	ON	OFF	+12V_DSW	Adaptor in
4	V_12V_DUAL1_MEM1/2	12V	ON	ON	ON	ON	ON	OFF	+12V/+12V_DSW	PS_PG_5V
5	+3P3V_AUX	3.3V	ON	ON	ON	ON	OFF	OFF	+3P3V/+3P3V_DSW	PCH_DEEPSLEEP_N/PS_PG_12V
6	+5V_AUX	5V	ON	ON	ON	ON	OFF	OFF	+12V_DSW	PCH:PCH_DEEPSLEEP_N
7	V_12V_DUAL_PCH	12V	ON	ON	ON	ON	ON	OFF	+12V/+12V_DSW	PS_PG_5V
8	+PGPPA_AUX_PCH	3.3V/1.8V	ON	ON	ON	ON	OFF	OFF	+3P3V_AUX	connect to +3P3V_AUX through 0 ohm resister
9	+1P0V_AUX_PCH	1.0V	ON	ON	ON	ON	OFF	OFF	V_12V_DUAL_PCH	CPLD(EC5055): VR_1P05V_PCH_EN
10	+3P3V_AUX_SLOT	3.3V	ON	ON	ON	ON	OFF	OFF	+12V_DSW	CPLD(EC5055): VR_3P3AUX_SLOT_EN
11	+3P3V_DSW_LAN	3.3V	ON	ON	ON	OFF	OFF	OFF	+3P3V_DSW	PCH:PCH_SLP_LAN_N
12	V_3VAUX_MEM_CPU0	3.3V	ON	ON	OFF	OFF	OFF	OFF	+3P3V_DSW	CPLD(EC5055): V_5VAUX_MEM_CPU0/1_EN_N
13	V_5VAUX_MEM_CPU0	5V	ON	ON	OFF	OFF	OFF	OFF	+5V_DSW	CPLD(EC5055): V_5VAUX_MEM_CPU0/1_EN_N
14	+5V_USBKB	5V	ON	ON	OFF	OFF	OFF	OFF	+5V/+5V_DSW	CPLD(EC5055): STBY_FROM_AUX_EN & PS_PG_12V
15	+VDDQ012/345_CPU0	1.2V	ON	ON	OFF	OFF	OFF	OFF	V_12V_DUAL1/2_MEM1/2	CPLD (EC5055) : VR_MEM_VDD_PVPP_CPU[1:0]_EN
16	+VPP012/345_CPU0	2.6V	ON	ON	OFF	OFF	OFF	OFF	V_12V_DUAL1/2_MEM1/2	CPLD (EC5055) : VR_MEM_VDD_PVPP_CPU[1:0]_EN
17	+VTT012/345_CPU0	1.2V	ON	ON	OFF	OFF	OFF	OFF	+VDDQ012/345_CPU0/1	MEM_VTT_DRVR_CPU0/1_EN
18	+12V	12V	ON	OFF	OFF	OFF	OFF	OFF	PSU	PS_ON
19	+VCORE_CPU0	1.8V	ON	OFF	OFF	OFF	OFF	OFF	+12V	CPLD (EC5055) : VR_CPU[1:0]_VCCIN_EN
20	+VCCSA_CPU0	1.8V	ON	OFF	OFF	OFF	OFF	OFF	+12V	CPLD (EC5055) : VR_CPU[1:0]_VCCIN_EN
21	+VCCIO_CPU0	1V	ON	OFF	OFF	OFF	OFF	OFF	+12V	CPLD (EC5055) : VR_CPU0/1_VCCIO_EN
22	+5V	5V	ON	OFF	OFF	OFF	OFF	OFF	+12V	CPLD (EC5055) : VR_MAIN_EN
23	+3P3V	3.3V	ON	OFF	OFF	OFF	OFF	OFF	+12V	CPLD (EC5048) :VR_3P3V_EN
24	+P2V5_CPU0	2.5V	ON	OFF	OFF	OFF	OFF	OFF	+VPP012_CPU0/1	CPLD (EC5055) : EM_SLPS3_P2V5_CPU0[1:0]_N
25	-12V	-12V	ON	OFF	OFF	OFF	OFF	OFF	PSU	PS_ON

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System Power Rail
Rev 0.1
Apr/19/2016

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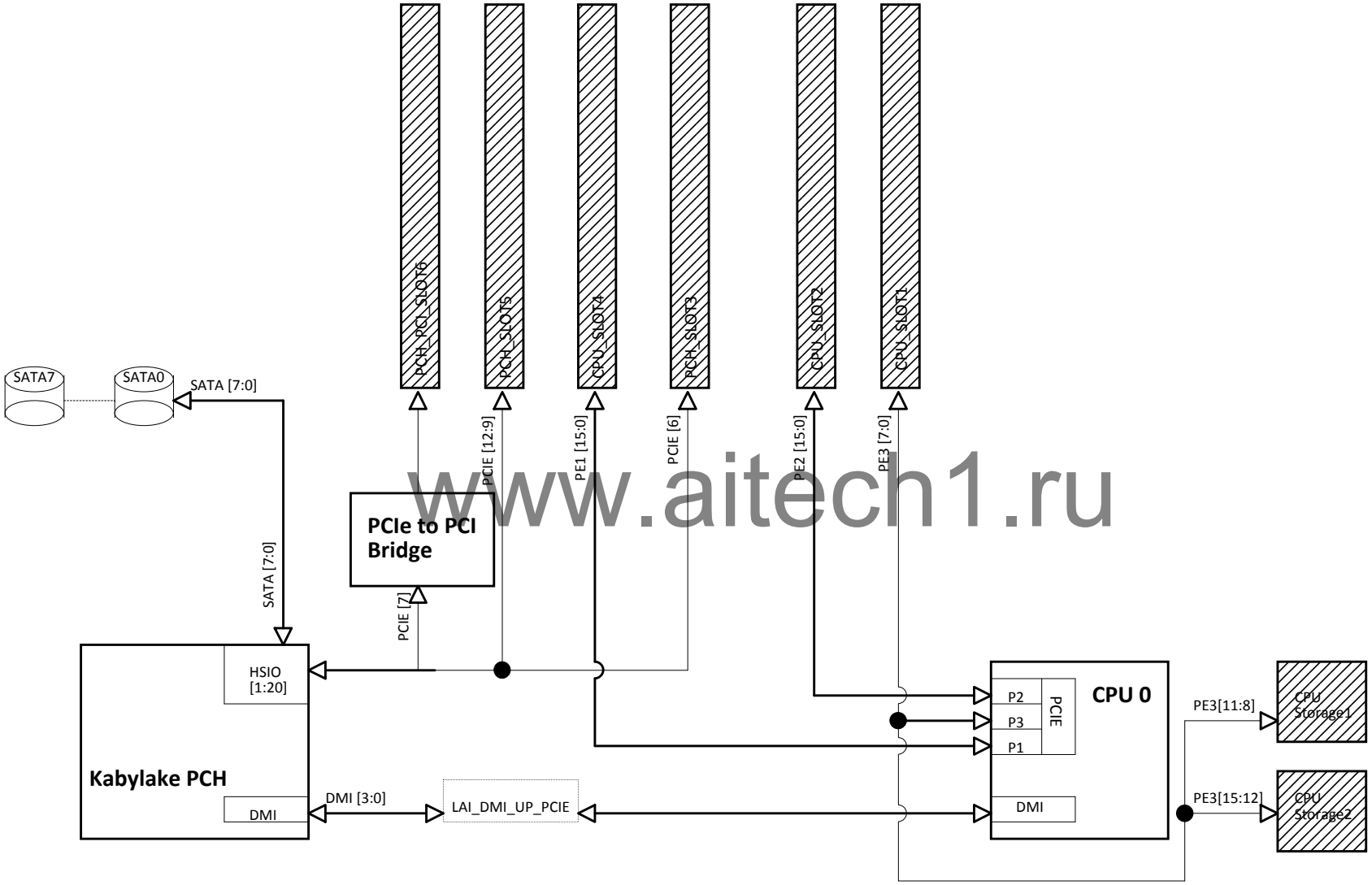
TITLE	System Power Rail		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	14 of 147

COMPRESSED IMAGE

Matira 3 PCIe Connection Diagram



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PCIe Connection Diagram
Rev 0.1
Apr/19/2016

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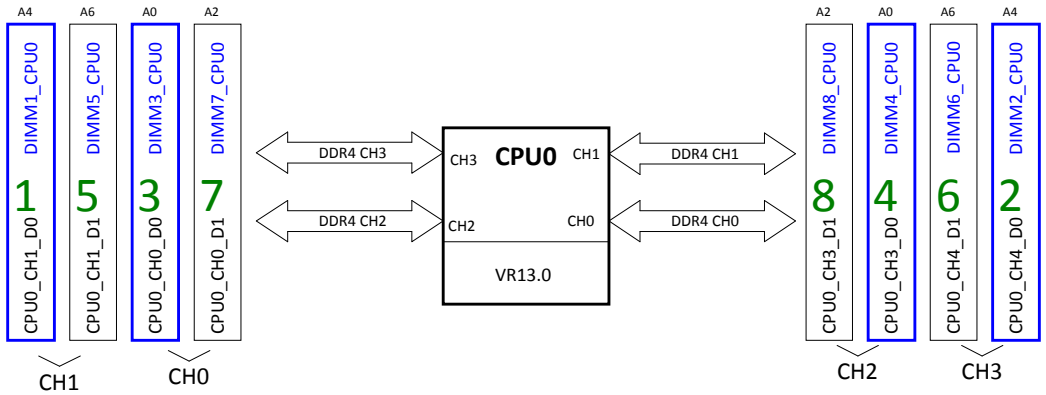
TITLE	PCIe Connection Diagram		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	15 of 147

COMPRESSED IMAGE

Matira 3 Memory Connection Diagram



White Ejector / Black Body

Black Ejector / Black Body

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SILKSCREEN	CHANNEL	DIMM	SA[2:0]	SPD	TSOD
DIMM3	0	0	000	0xA0	0x30
DIMM7		1	001	0xA2	0x32
DIMM1	1	0	010	0xA4	0x34
DIMM5		1	011	0xA6	0x36
DIMM4	2	0	000	0xA0	0x30
DIMM8		1	001	0xA2	0x32
DIMM2	3	0	010	0xA4	0x34
DIMM6		1	011	0xA6	0x36

Memory Connection Diagram
Rev 0.1
Apr/19/2016

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TITLE Memory Connection Diagram
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TITLE	BLANK		
DWG NO.	MATIRA 3	REV.	A00
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COMPRESSED IMAGE

Matira3 PCB Stackup

Foxconn stackup design

Layer NO.	Layer Name	Min. layer thickness (mil)	Typical layer thickness (mil)	Max. layer thickness (mil)	Dielectric Constant	Remark
	Solder Mask	0.40	0.50	1.80	3.70	
L1	Signal	1.40	1.90	2.40	NA	1.5 oz¡]with. Plating)
	Prepreg	2.20	2.70	3.30	3.90	
L2	Power/Gnd	1.00	1.30	1.40	NA	1 oz
	Core	3.50	4.00	4.50	3.90	
L3	Signal	1.00	1.30	1.40	NA	1 oz
	Prepreg	NA	15.00	NA	3.90	
L4	Power/Gnd	2.20	2.60	2.60	NA	2 oz
	Core	4.00	4.00	6.00	3.90	
L5	Power/Gnd	2.20	2.60	2.60	NA	2 oz
	Prepreg	NA	15.00	NA	3.90	
L6	Signal	1.00	1.30	1.40	NA	1 oz
	Core	3.50	4.00	4.50	3.90	
L7	Power/Gnd	1.00	1.30	1.40	NA	1 oz
	Prepreg	2.20	2.70	3.20	3.90	
L8	Signal	1.40	1.90	2.40	NA	1.5 oz¡]with. Plating)
	Solder Mask	0.40	0.50	1.80	3.70	
Total thickness			**62.60**			

Solder Mask	Min.	Typical	Max.
Solder Mask (a)	0.4 mil	1.9 mil	2.4 mil
Solder Mask (b, d)	0.4 mil		
Solder Mask (c)	0.4 mil	0.5 mil	1.8 mil

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Notes :

*2: Spacing of plane 4 to plane 5 must be 4 to 6 mils

*3: Spacing of layer 3 to plane 4 must be at least 3x the distance of plane 2 to layer 3 (similarly w/ layer 6 and planes 5 & 7)

*4: Thickness spec.: 63 +/-6 mils

PCB Thickness : 63 mils

PCB Thickness Tolerance : +8/- 5 mils

Impedance Calculation

COMPRESSED IMAGE

PCB Stackup
Rev 0.1
Apr/19/2016

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TITLE	PCB Stackup		
DWG NO.	MATIRA 3	REV.	A00
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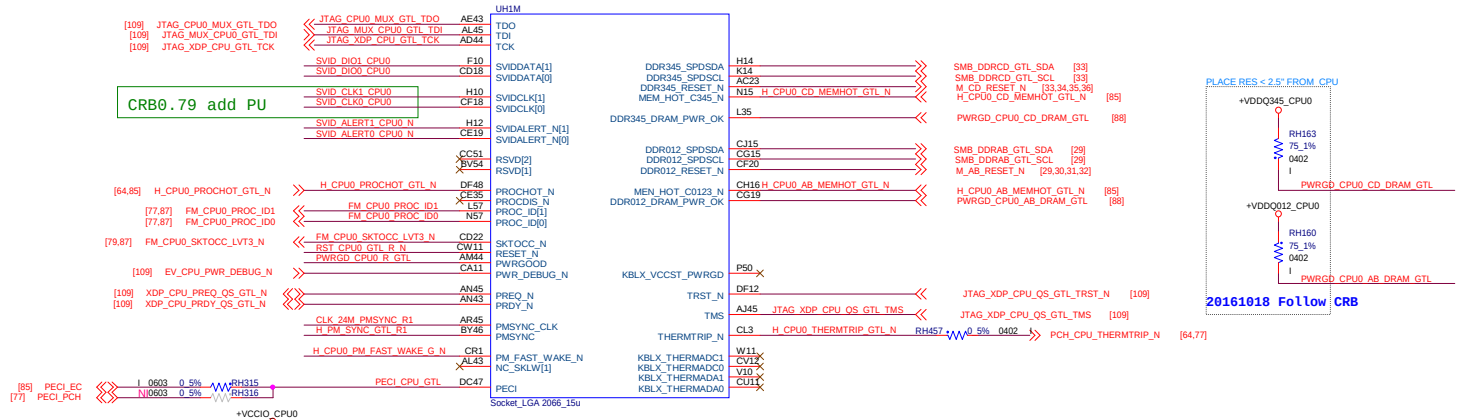
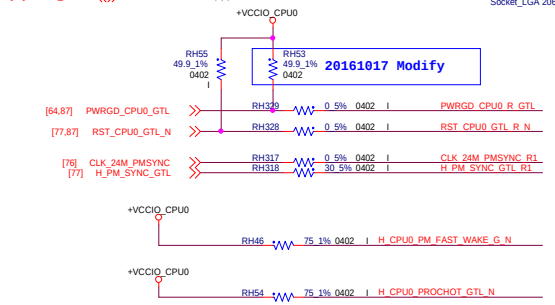
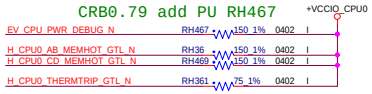
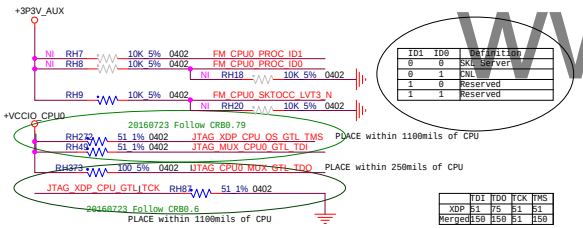
COMPRESSED IMAGE









ID1	ID0	Definition
0	0	SKL Server
0	1	CNL
1	0	Reserved
1	1	Reserved

	TDI	TDO	TCK	TMS
XDP	51	75	51	51
Merged	150	150	51	150

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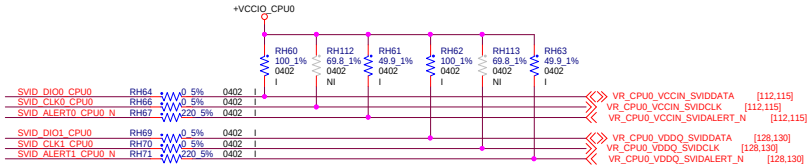
Follow PDG0.7



PDG0.7

	SVID_DATA/Series	SVID_CLK/Series	SVID_ALERT/Series
CPU SIDE	100/0	NI/0	49.9/220
Controller Side	100/0	49.9/150	NI/0

CRB0.79

	SVID_DATA/Series	SVID_CLK/Series	SVID_ALERT/Series
CPU SIDE	240/0	69.8(NI)/0	100/0
Controller Side	240/0	69.8/150	0(NI)/0

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TITLE CPU0 Misc
DWG NO. MATIRA 3
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DDR4_CHA

[29,30] M_A_DQ_[63..0]

UH1A

M_A_DQ_0	CA3	DDR0_DQ[0]	
M_A_DQ_1	CC3	DDR0_DQ[1]	
M_A_DQ_2	CG5	DDR0_DQ[2]	
M_A_DQ_3	CJ5	DDR0_DQ[3]	
M_A_DQ_4	CA5	DDR0_DQ[4]	
M_A_DQ_5	CC5	DDR0_DQ[5]	
M_A_DQ_6	CG3	DDR0_DQ[6]	
M_A_DQ_7	CJ3	DDR0_DQ[7]	
M_A_DQ_8	CR5	DDR0_DQ[8]	
M_A_DQ_9	CN3	DDR0_DQ[9]	
M_A_DQ_10	CV4	DDR0_DQ[10]	
M_A_DQ_11	CW3	DDR0_DQ[11]	
M_A_DQ_12	CM4	DDR0_DQ[12]	
M_A_DQ_13	CN5	DDR0_DQ[13]	
M_A_DQ_14	CY2	DDR0_DQ[14]	
M_A_DQ_15	CV2	DDR0_DQ[15]	
M_A_DQ_16	DA7	DDR0_DQ[16]	
M_A_DQ_17	DE7	DDR0_DQ[17]	
M_A_DQ_18	DB10	DDR0_DQ[18]	
M_A_DQ_19	DD10	DDR0_DQ[19]	
M_A_DQ_20	DB6	DDR0_DQ[20]	
M_A_DQ_21	DD6	DDR0_DQ[21]	
M_A_DQ_22	DA9	DDR0_DQ[22]	
M_A_DQ_23	DE9	DDR0_DQ[23]	
M_A_DQ_24	DD12	DDR0_DQ[24]	
M_A_DQ_25	DE13	DDR0_DQ[25]	
M_A_DQ_26	DB16	DDR0_DQ[26]	
M_A_DQ_27	DD16	DDR0_DQ[27]	
M_A_DQ_28	DA13	DDR0_DQ[28]	
M_A_DQ_29	DB12	DDR0_DQ[29]	
M_A_DQ_30	DE15	DDR0_DQ[30]	
M_A_DQ_31	DA15	DDR0_DQ[31]	
M_A_DQ_32	DA37	DDR0_DQ[32]	
M_A_DQ_33	DE37	DDR0_DQ[33]	
M_A_DQ_34	DD40	DDR0_DQ[34]	
M_A_DQ_35	DB40	DDR0_DQ[35]	
M_A_DQ_36	DB36	DDR0_DQ[36]	
M_A_DQ_37	DD36	DDR0_DQ[37]	
M_A_DQ_38	DE39	DDR0_DQ[38]	
M_A_DQ_39	DA39	DDR0_DQ[39]	
M_A_DQ_40	DA43	DDR0_DQ[40]	
M_A_DQ_41	DE43	DDR0_DQ[41]	
M_A_DQ_42	DB46	DDR0_DQ[42]	
M_A_DQ_43	DA45	DDR0_DQ[43]	
M_A_DQ_44	DD42	DDR0_DQ[44]	
M_A_DQ_45	DB42	DDR0_DQ[45]	
M_A_DQ_46	DE45	DDR0_DQ[46]	
M_A_DQ_47	DD46	DDR0_DQ[47]	
M_A_DQ_48	CU45	DDR0_DQ[48]	
M_A_DQ_49	CV46	DDR0_DQ[49]	
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M_A_DQ_51	CR49	DDR0_DQ[51]	
M_A_DQ_52	CP46	DDR0_DQ[52]	
M_A_DQ_53	CR45	DDR0_DQ[53]	
M_A_DQ_54	CV48	DDR0_DQ[54]	
M_A_DQ_55	CP48	DDR0_DQ[55]	
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M_A_DQ_57	DA49	DDR0_DQ[57]	
M_A_DQ_58	DB52	DDR0_DQ[58]	
M_A_DQ_59	DA51	DDR0_DQ[59]	
M_A_DQ_60	DD48	DDR0_DQ[60]	
M_A_DQ_61	DB48	DDR0_DQ[61]	
M_A_DQ_62	DE51	DDR0_DQ[62]	
M_A_DQ_63	DD52	DDR0_DQ[63]	

		DDR0_DQS_DP[0]	CH4
		DDR0_DQS_DN[0]	CF4
		DDR0_DQS_DP[1]	CU5
		DDR0_DQS_DN[1]	CT4
		DDR0_DQS_DP[2]	DF8
		DDR0_DQS_DN[2]	DD8
		DDR0_DQS_DP[3]	DD14
		DDR0_DQS_DN[3]	DB38
		DDR0_DQS_DP[4]	CY38
		DDR0_DQS_DN[4]	CY44
		DDR0_DQS_DP[5]	DB44
		DDR0_DQS_DN[5]	CR47
		DDR0_DQS_DP[6]	CN47
		DDR0_DQS_DN[6]	CY50
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		DDR0_DQS_DN[7]	DB20
		DDR0_DQS_DP[8]	DA21
		DDR0_DQS_DN[8]	CB4
		DDR0_DQS_DP[9]	CD4
		DDR0_DQS_DN[9]	CR3
		DDR0_DQS_DP[10]	CP2
		DDR0_DQS_DN[10]	CY8
		DDR0_DQS_DP[11]	DB8
		DDR0_DQS_DN[11]	CY14
		DDR0_DQS_DP[12]	DB14
		DDR0_DQS_DN[12]	DD38
		DDR0_DQS_DP[13]	DF38
		DDR0_DQS_DN[13]	DD44
		DDR0_DQS_DP[14]	DF44
		DDR0_DQS_DN[14]	CU47
		DDR0_DQS_DP[15]	CW47
		DDR0_DQS_DN[15]	DD50
		DDR0_DQS_DP[16]	DF50
		DDR0_DQS_DN[16]	DD18
		DDR0_DQS_DP[17]	DC19
		DDR0_DQS_DN[17]	

M_A_DQS_DP_0	[29,30]		
M_A_DQS_DN_0	[29,30]		
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M_A_DQS_DP_13	[29,30]		
M_A_DQS_DN_13	[29,30]		
M_A_DQS_DP_14	[29,30]		
M_A_DQS_DN_14	[29,30]		
M_A_DQS_DP_15	[29,30]		
M_A_DQS_DN_15	[29,30]		
M_A_DQS_DP_16	[29,30]		
M_A_DQS_DN_16	[29,30]		
M_A_DQS_DP_17	[29,30]		
M_A_DQS_DN_17	[29,30]		

		CW19	M_A_ECC_0
		CY20	M_A_ECC_1
		DE21	M_A_ECC_2
		DF20	M_A_ECC_3
		CY18	M_A_ECC_4
		DB18	M_A_ECC_5
		DC21	M_A_ECC_6
		DE20	M_A_ECC_7

M_A_ECC_[7..0] [29,30]

Socket_LGA 2066_15u

DDR4_CHB

[31,32] M_B_DQ_[63..0]

UH1B

M_B_DQ_0	CA7	DDR1_DQ[0]	
M_B_DQ_1	CC7	DDR1_DQ[1]	
M_B_DQ_2	CD10	DDR1_DQ[2]	
M_B_DQ_3	CF10	DDR1_DQ[3]	
M_B_DQ_4	CA9	DDR1_DQ[4]	
M_B_DQ_5	BY8	DDR1_DQ[5]	
M_B_DQ_6	CF8	DDR1_DQ[6]	
M_B_DQ_7	CG9	DDR1_DQ[7]	
M_B_DQ_8	CR7	DDR1_DQ[8]	
M_B_DQ_9	CU7	DDR1_DQ[9]	
M_B_DQ_10	CL9	DDR1_DQ[10]	
M_B_DQ_11	CM10	DDR1_DQ[11]	
M_B_DQ_12	CJ7	DDR1_DQ[12]	
M_B_DQ_13	CL7	DDR1_DQ[13]	
M_B_DQ_14	CR9	DDR1_DQ[14]	
M_B_DQ_15	CP10	DDR1_DQ[15]	
M_B_DQ_16	CK12	DDR1_DQ[16]	
M_B_DQ_17	CM12	DDR1_DQ[17]	
M_B_DQ_18	CN15	DDR1_DQ[18]	
M_B_DQ_19	CR15	DDR1_DQ[19]	
M_B_DQ_20	CJ13	DDR1_DQ[20]	
M_B_DQ_21	CK14	DDR1_DQ[21]	
M_B_DQ_22	CR13	DDR1_DQ[22]	
M_B_DQ_23	CT14	DDR1_DQ[23]	
M_B_DQ_24	CD12	DDR1_DQ[24]	
M_B_DQ_25	CE13	DDR1_DQ[25]	
M_B_DQ_26	CA15	DDR1_DQ[26]	
M_B_DQ_27	CB16	DDR1_DQ[27]	
M_B_DQ_28	CB12	DDR1_DQ[28]	
M_B_DQ_29	CA13	DDR1_DQ[29]	
M_B_DQ_30	CE15	DDR1_DQ[30]	
M_B_DQ_31	CD16	DDR1_DQ[31]	
M_B_DQ_32	CK36	DDR1_DQ[32]	
M_B_DQ_33	CL37	DDR1_DQ[33]	
M_B_DQ_34	CG39	DDR1_DQ[34]	
M_B_DQ_35	CH40	DDR1_DQ[35]	
M_B_DQ_36	CH36	DDR1_DQ[36]	
M_B_DQ_37	CG37	DDR1_DQ[37]	
M_B_DQ_38	CL39	DDR1_DQ[38]	
M_B_DQ_39	CK40	DDR1_DQ[39]	
M_B_DQ_40	CU39	DDR1_DQ[40]	
M_B_DQ_41	CV40	DDR1_DQ[41]	
M_B_DQ_42	CP42	DDR1_DQ[42]	
M_B_DQ_43	CR43	DDR1_DQ[43]	
M_B_DQ_44	CR39	DDR1_DQ[44]	
M_B_DQ_45	CP40	DDR1_DQ[45]	
M_B_DQ_46	CV42	DDR1_DQ[46]	
M_B_DQ_47	CU43	DDR1_DQ[47]	
M_B_DQ_48	CK42	DDR1_DQ[48]	
M_B_DQ_49	CL43	DDR1_DQ[49]	
M_B_DQ_50	CH46	DDR1_DQ[50]	
M_B_DQ_51	CG45	DDR1_DQ[51]	
M_B_DQ_52	CH42	DDR1_DQ[52]	
M_B_DQ_53	CG43	DDR1_DQ[53]	
M_B_DQ_54	CL46	DDR1_DQ[54]	
M_B_DQ_55	CK46	DDR1_DQ[55]	
M_B_DQ_56	CL51	DDR1_DQ[56]	
M_B_DQ_57	CJ51	DDR1_DQ[57]	
M_B_DQ_58	CH48	DDR1_DQ[58]	
M_B_DQ_59	CF48	DDR1_DQ[59]	
M_B_DQ_60	CM50	DDR1_DQ[60]	
M_B_DQ_61	CL49	DDR1_DQ[61]	
M_B_DQ_62	CF50	DDR1_DQ[62]	
M_B_DQ_63	CE49	DDR1_DQ[63]	

		CB10	M_B_DQS_DP_0
		CC9	M_B_DQS_DN_0
		CP8	M_B_DQS_DP_1
		CT8	M_B_DQS_DN_1
		CN13	M_B_DQS_DP_2
		CP12	M_B_DQS_DN_2
		BY14	M_B_DQS_DP_3
		CB14	M_B_DQS_DN_3
		CF38	M_B_DQS_DP_4
		CH38	M_B_DQS_DN_4
		CR41	M_B_DQS_DP_5
		CN41	M_B_DQS_DN_5
		CH44	M_B_DQS_DP_6
		CF44	M_B_DQS_DN_6
		CH50	M_B_DQS_DP_7
		CG51	M_B_DQS_DN_7
		CM18	M_B_DQS_DP_8
		CK18	M_B_DQS_DN_8
		CD8	M_B_DQS_DP_9
		CE7	M_B_DQS_DN_9
		CM8	M_B_DQS_DP_10
		CK8	M_B_DQS_DN_10
		CM14	M_B_DQS_DP_11
		CL15	M_B_DQS_DN_11
		CD14	M_B_DQS_DP_12
		CF14	M_B_DQS_DN_12
		CK38	M_B_DQS_DP_13
		CM38	M_B_DQS_DN_13
		CU41	M_B_DQS_DP_14
		CW41	M_B_DQS_DN_14
		CK44	M_B_DQS_DP_15
		CM44	M_B_DQS_DN_15
		CJ49	M_B_DQS_DP_16
		CK48	M_B_DQS_DN_16
		CP18	M_B_DQS_DP_17
		CT18	M_B_DQS_DN_17

		CR17	M_B_ECC_0
		CU17	M_B_ECC_1
		CL19	M_B_ECC_2
		CM20	M_B_ECC_3
		CJ17	M_B_ECC_4
		CL17	M_B_ECC_5
		CR19	M_B_ECC_6
		CP20	M_B_ECC_7

M_B_ECC_[7..0] [31,32]

Socket_LGA 2066_15u

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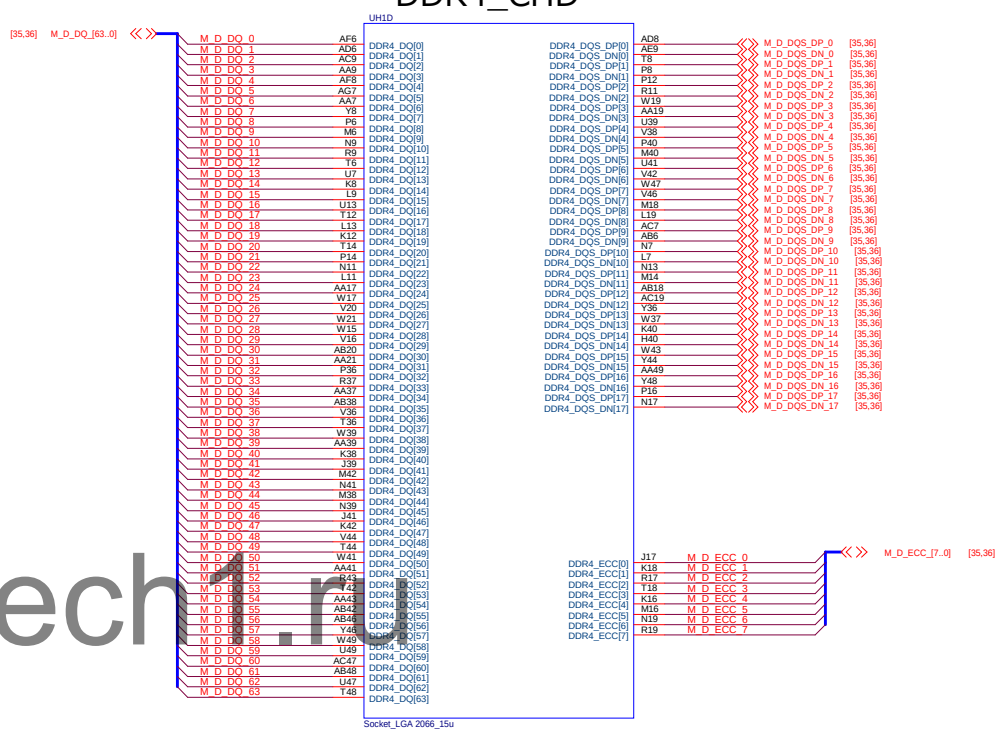
TITLE	CPU0 DDR4 CHA/CHB		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	20 of 147

COMPRESSED IMAGE

DDR4_CHC

DDR4_CHD



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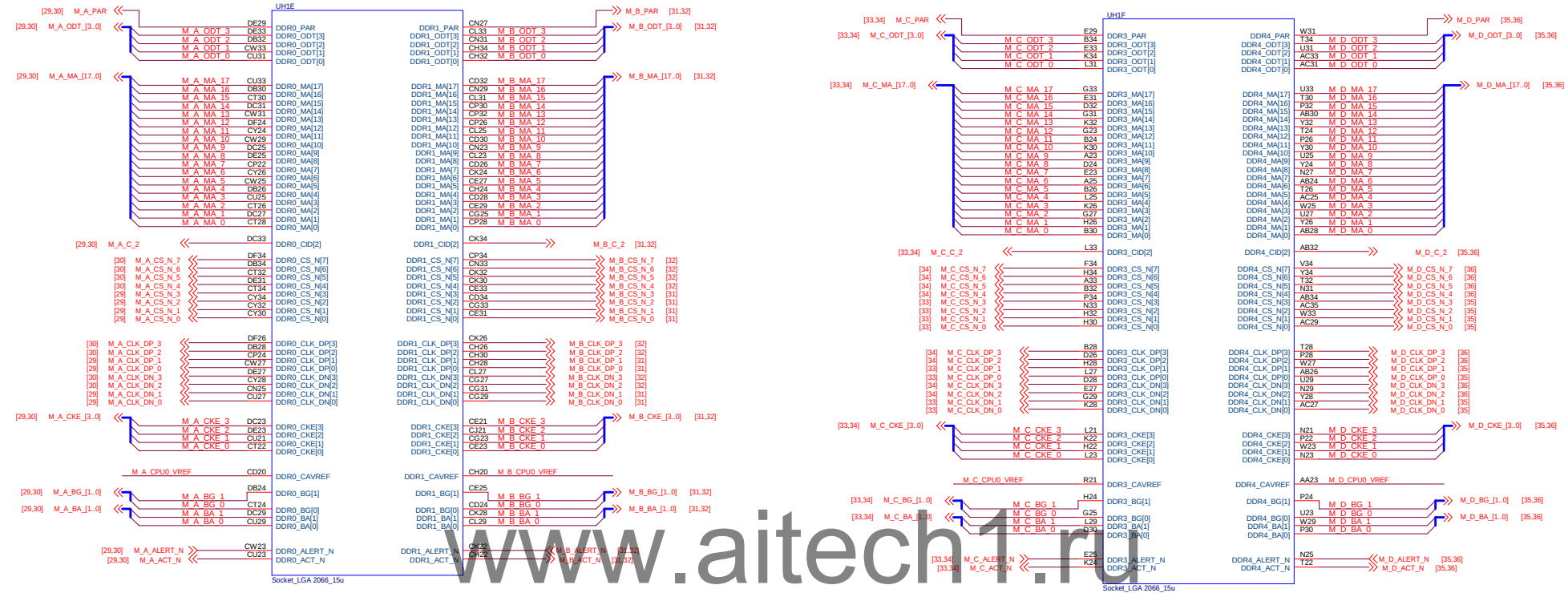
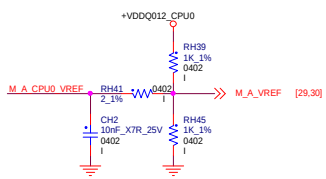
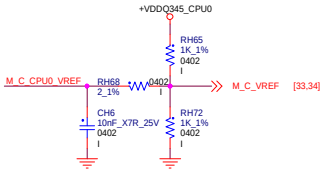
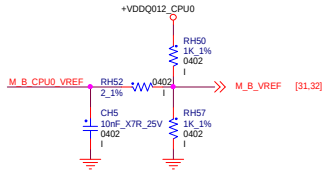
TITLE	CPU0 DDR4 CHC/CHD		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	21 of 147

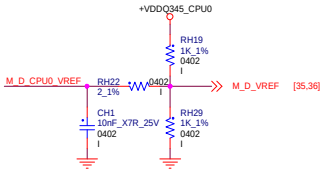
COMPRESSED IMAGE











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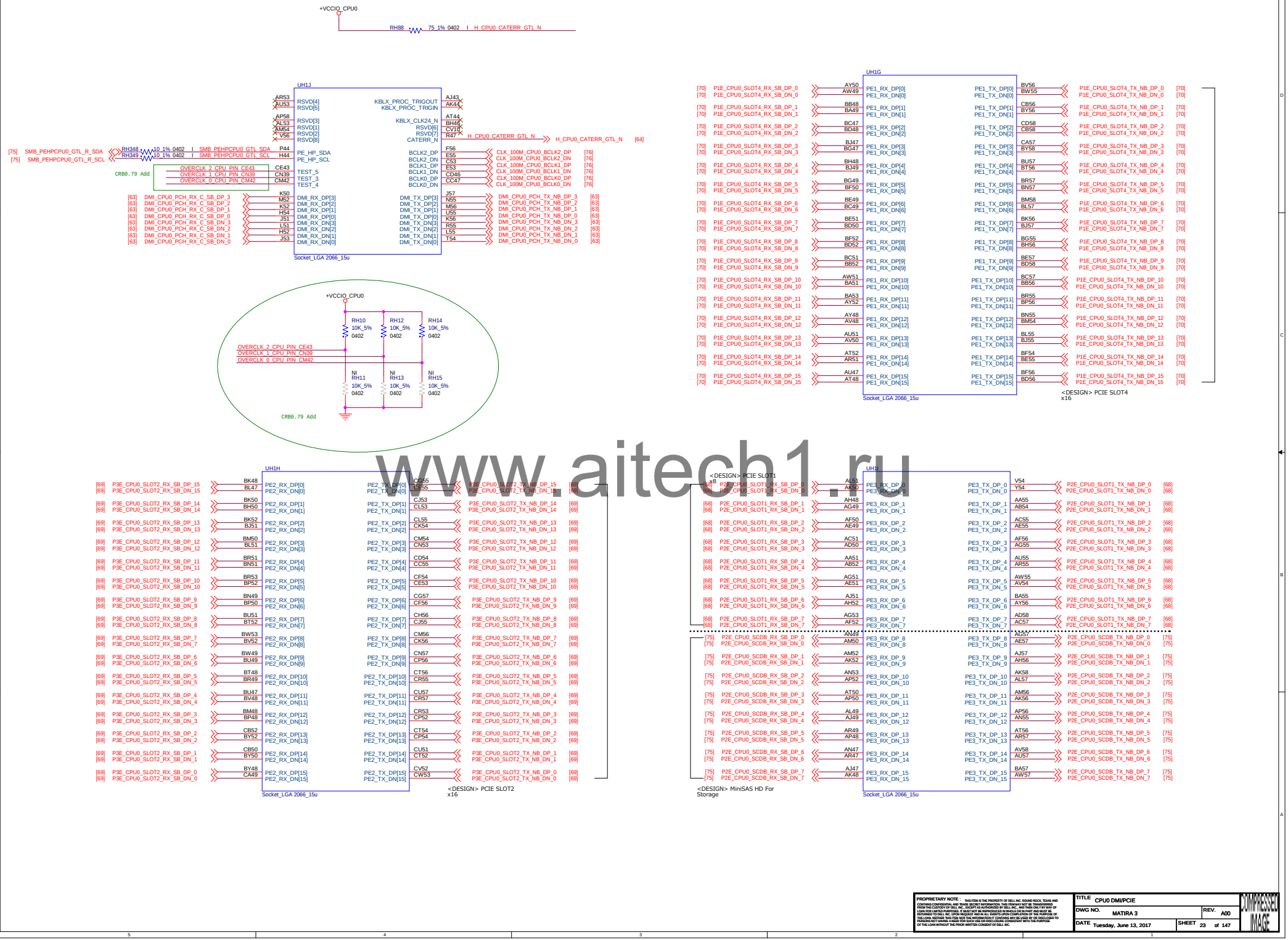
TITLE	CPU0 DDR4 CMD AND SIGNALS		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	22 of 147

CONFIDENTIAL IMAGE



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TITLE	CPU0 DMI/PCIE		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	23 of 147

COMPRESSED IMAGE

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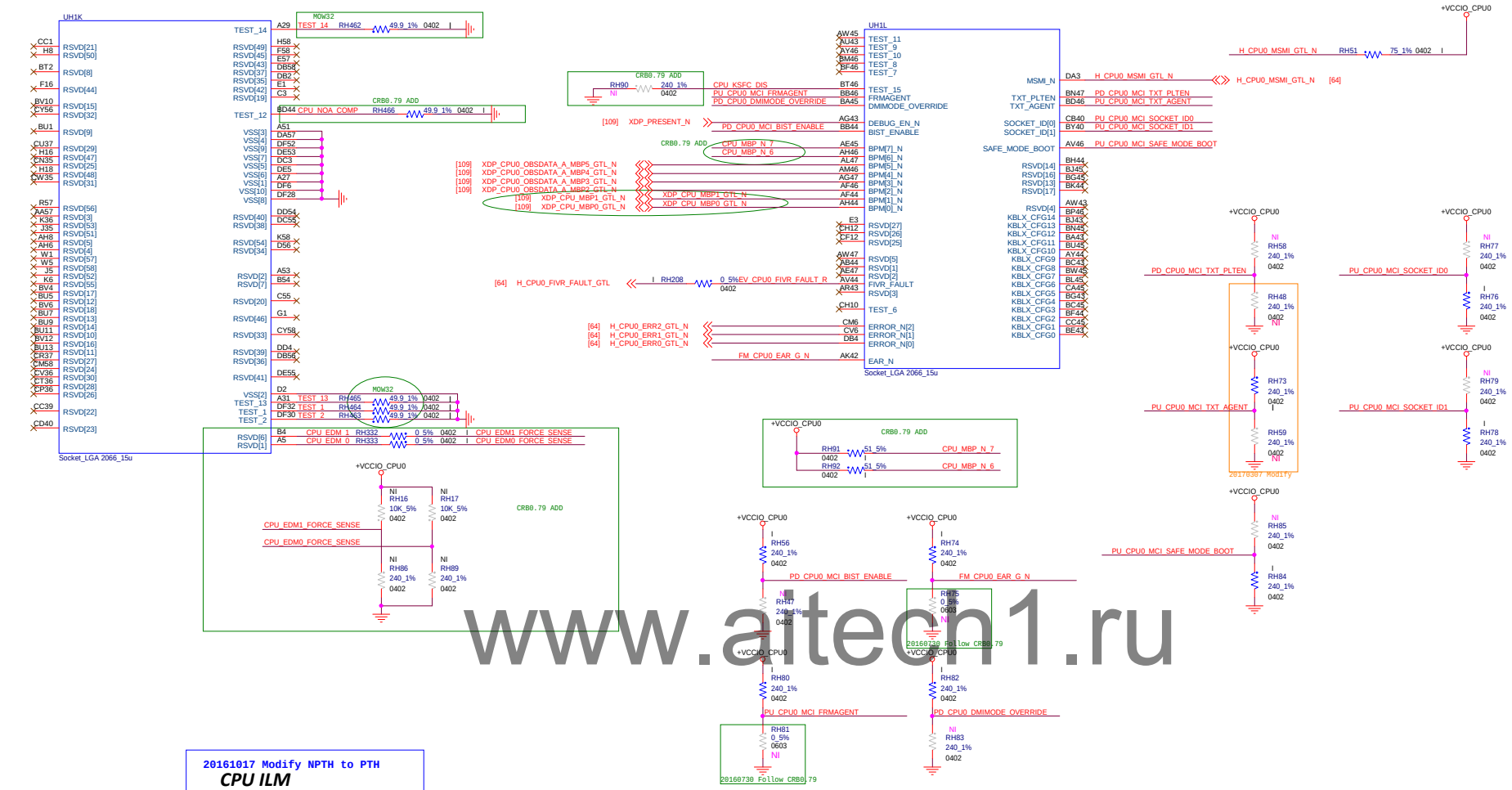
TITLE: BLANK			AITECH INC.
DWG NO. MATRIA.3	REV. A00		
DATE: Tuesday, June 13, 2017	SHEET 24 of 147		



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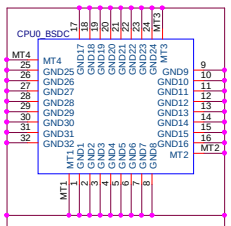
20161017 Modify NPTH to PTH

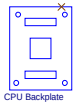
CPU ILM

PT44L12-471D



Narrow Back Plate

PT44P41-440D



CPU Backplate

CPU0_BP

MH13 NOBOM Mounting Hole — NP177

MH14 NOBOM Mounting Hole — NP177

20160822 Add for CPU heatsink hole base on SE's request

MH15 NOBOM Mounting Hole — NP177

MH16 NOBOM Mounting Hole — NP177

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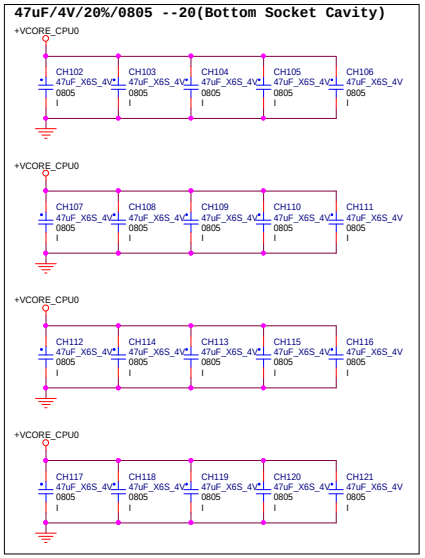
TITLE	CPU0 Test/Rsvd		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	25 of 147

COMPRESSED IMAGE

CPU0 VccIN VR13.0 Output Caps

330uF/2.5V/20%/Alum/7343 --7(VR's output-bottom)
47uF/4V/20%/0805 --20(Bottom Socket Cavity)
22uF/4V/20%/X6S/0805 -- 21(Top Socket Cavity)+10 (VR's output-bottom)



VCCIN CAP Count	CRB 0.79	PDG 0.7
TOP	21 (47uF)	21 (22uF)
BOT	20 (47uF)	20 (47uF)

COMPRESSED IMAGE

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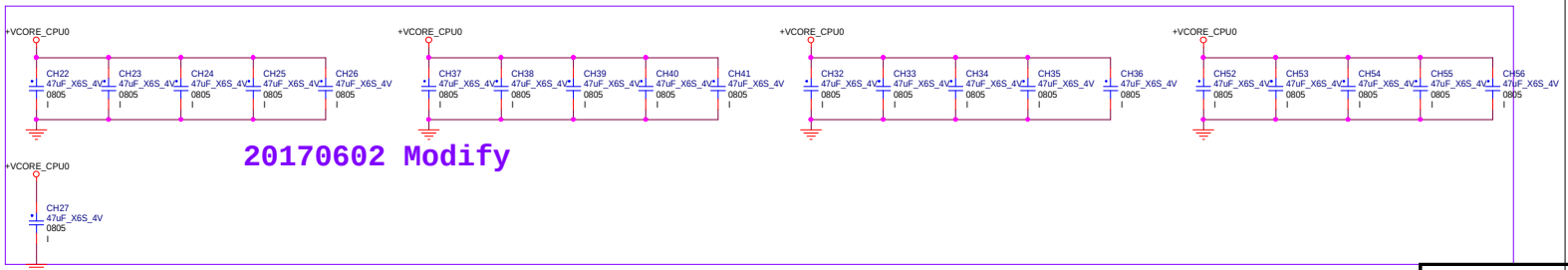
CPU0 VccIN VR13.0 Output Caps (Top Socket Cavity)



20170602 Modify

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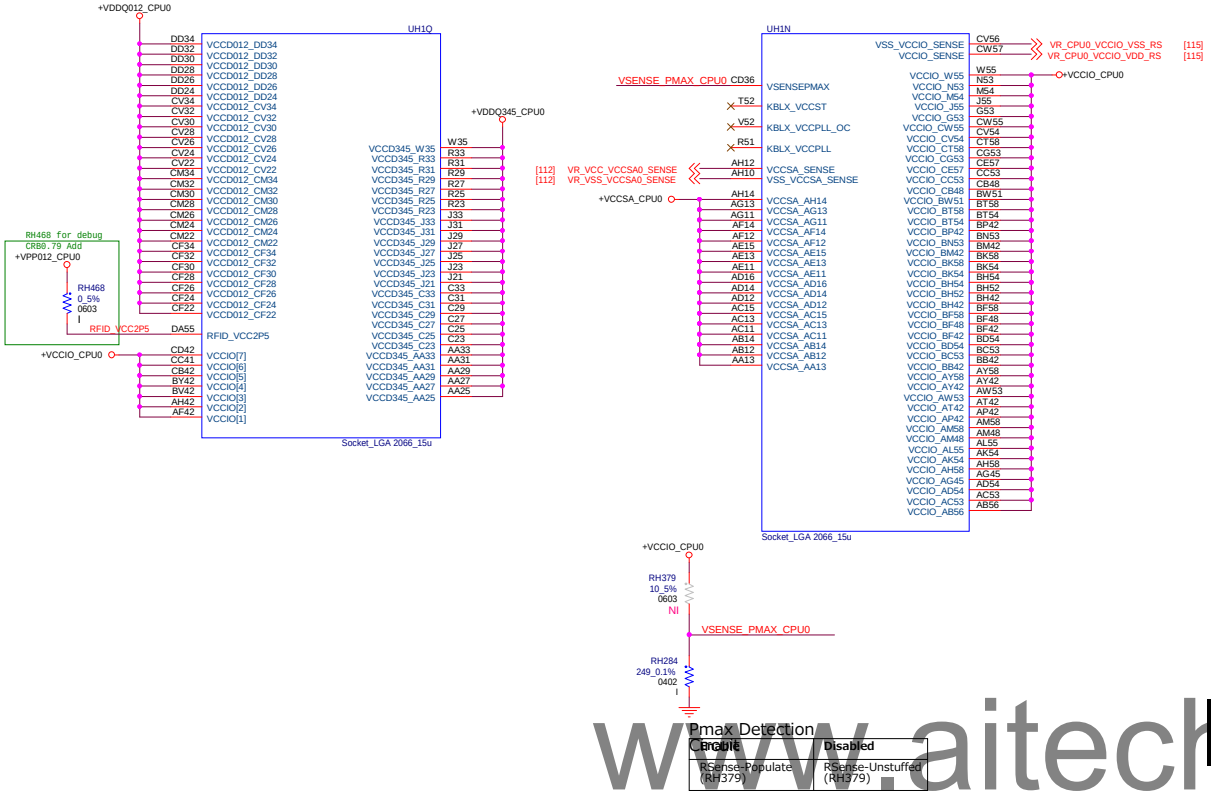
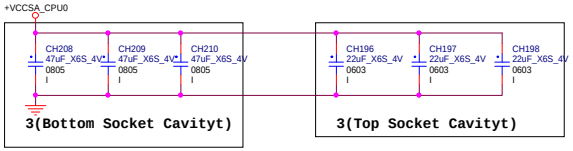
TITLE	CPU0 PWR-VCCIN		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	26 of 147

COMPRESSED IMAGE



CPU0 PVCCSA VR Decoupling Caps

66uF/4V/0V/20%/Alum/3018 --2(VR-bot)
22uF/4V/20%/X6S/0603 -- 2(VR-bot)+3(Top Socket Cavity)
47uF/6.3V/20%/X6S/0805 -- 3(Bottom Socket Cavity)



COMPRESSED IMAGE

VSA CAP Count	CRB 0.79	PDG 0.7
TOP	3 (47uF)	3 (22uF)
BOT	3 (47uF)	3 (47uF)

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Pmax Detection Caps

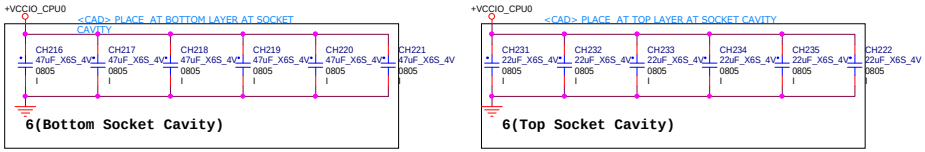
Enable	Disabled
RSense-Populate (RH379)	RSense-Unstuffed (RH379)

COMPRESSED IMAGE

VCCIO CAP Count	CRB 0.79	PDG 0.7
TOP	6 (47uF)	6 (22uF)
BOT	6 (47uF)	6 (47uF)

CPU0 PVCCIO Decoupling Caps

67uF/4V/0V/20%/Alum/3018 --2(VR-bot)
47uF/4V/20%/X6S/0805 -- 6(Bottom Socket Cavity)+3(VR-Top)
22uF/4V/20%/X6S/0805 -- 6(Top Socket Cavity)
10uF/6.3V/20%/X6S/0603 -- 2(VR-Top)



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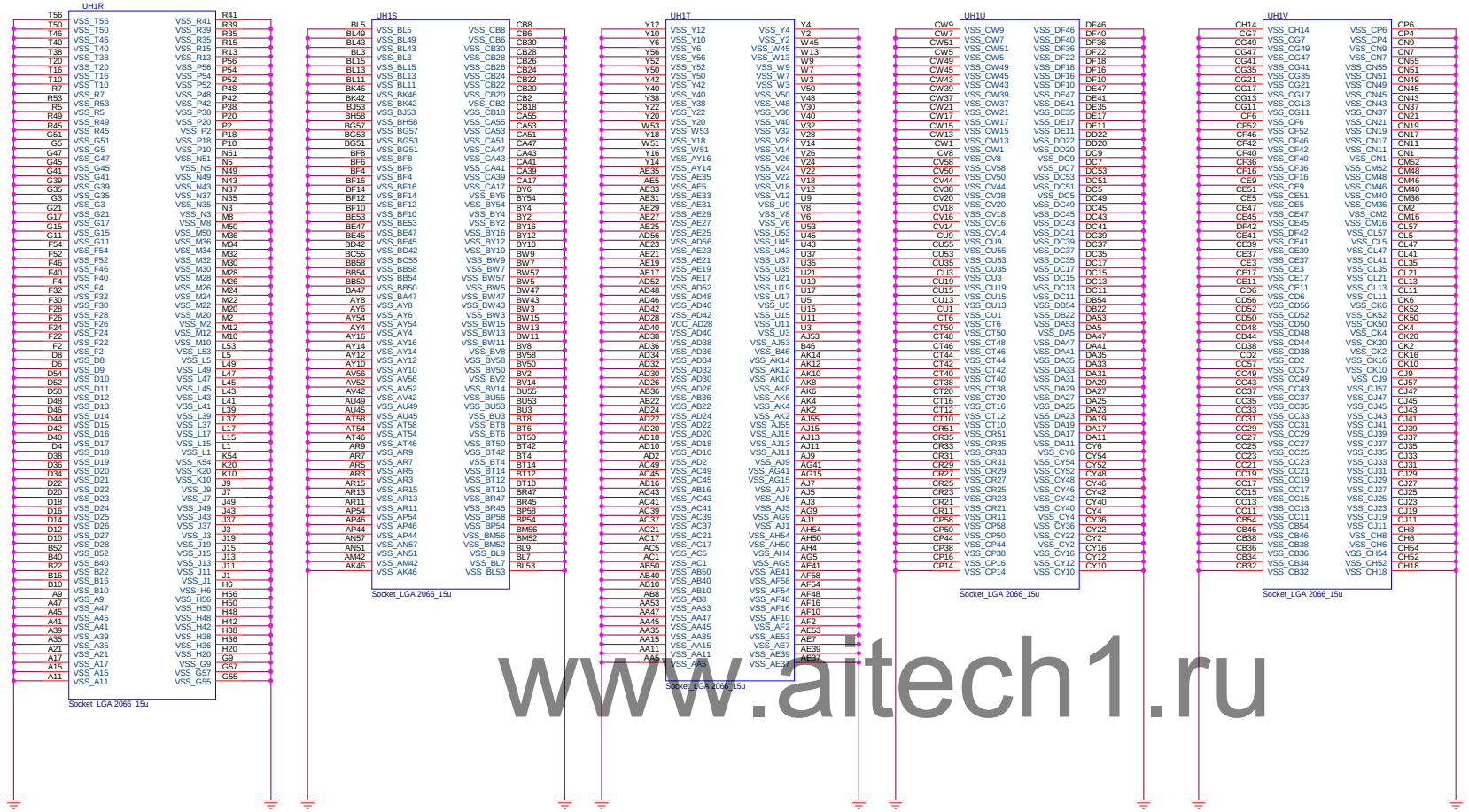
TITLE	CPU0 PWR-VCCD/VCCIO/VSA		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	27 of 147

COMPRESSED IMAGE



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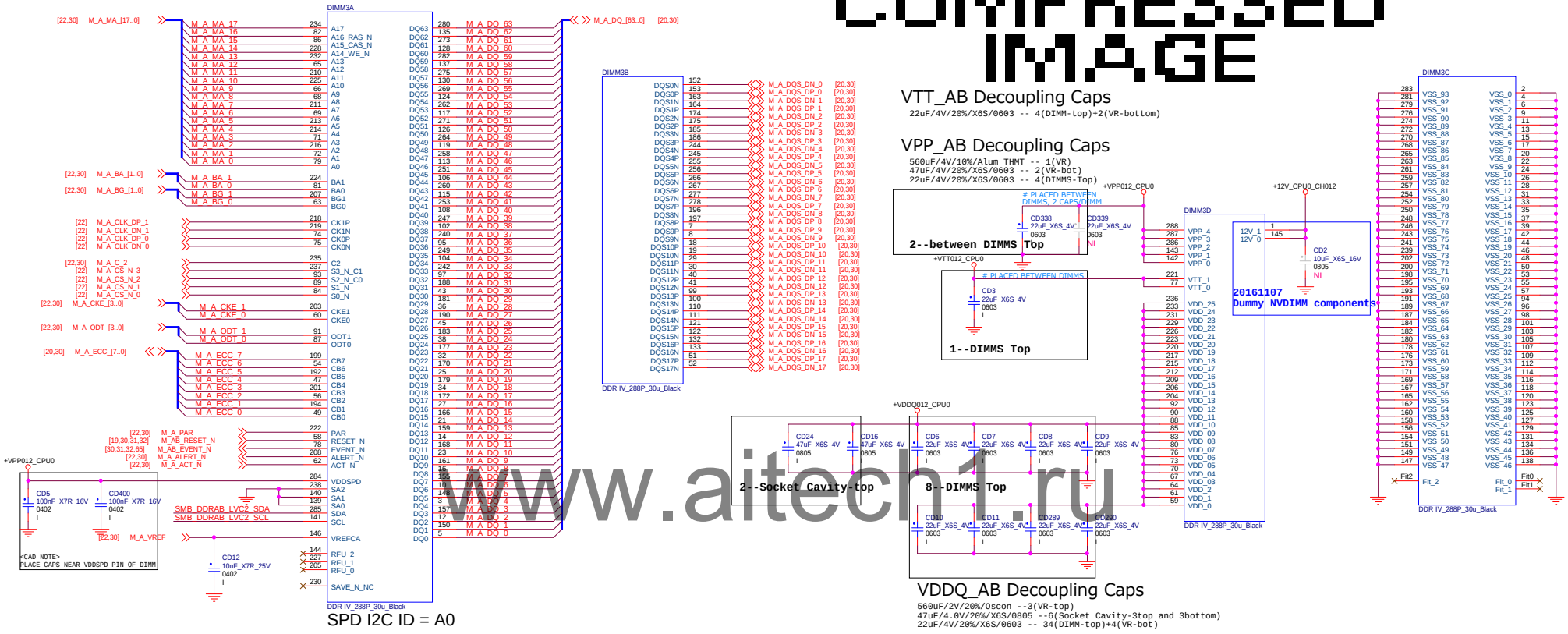
TITLE	CPU0 Ground		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	28 of 147

J-IMPRESSED IMAGE

SA[2:0] = 000
SPD = 0xA0
TSOD = 0x30

DDR4 DIMM3 CPU0.CHA.D0



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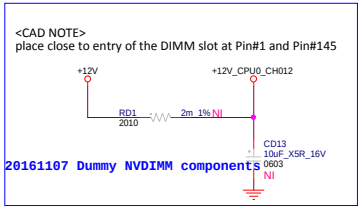

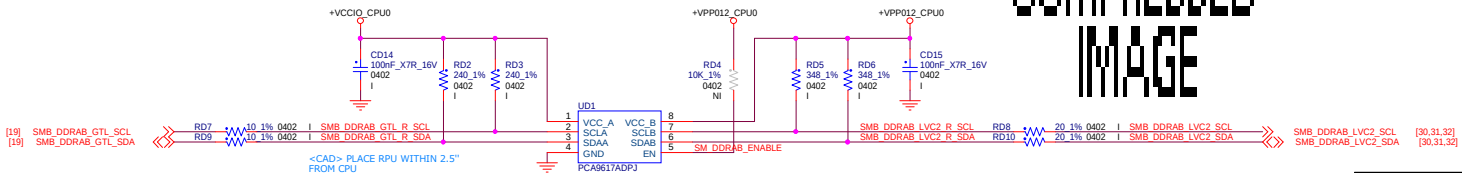

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TITLE	DDR4 DIMM3 CPU0.CHA.D0		
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DATE	Tuesday, June 13, 2017	SHEET	29 of 147

COMPRESSED IMAGE

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TSOD = 0x38

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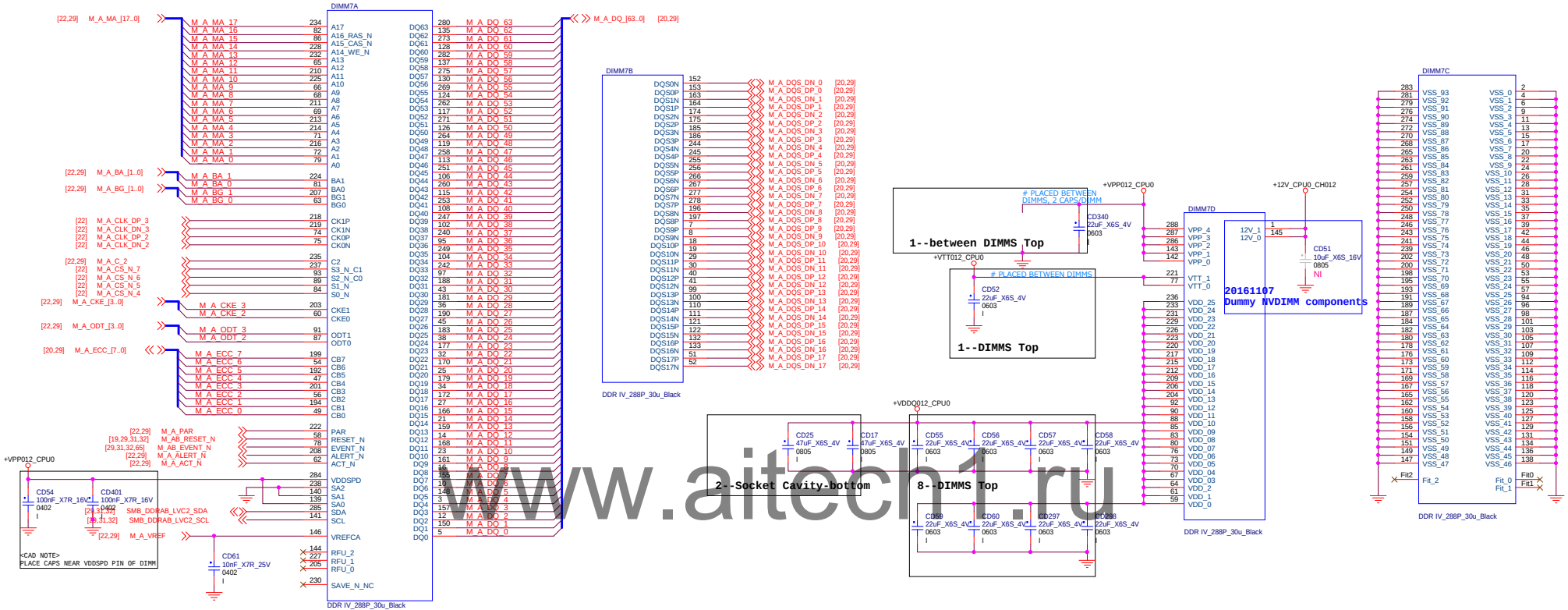

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TITLE	DDR4 DIMM7 CPU0.CHA.D1		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	30 of 147

COMPRESSED IMAGE

SA[2:0] = 010
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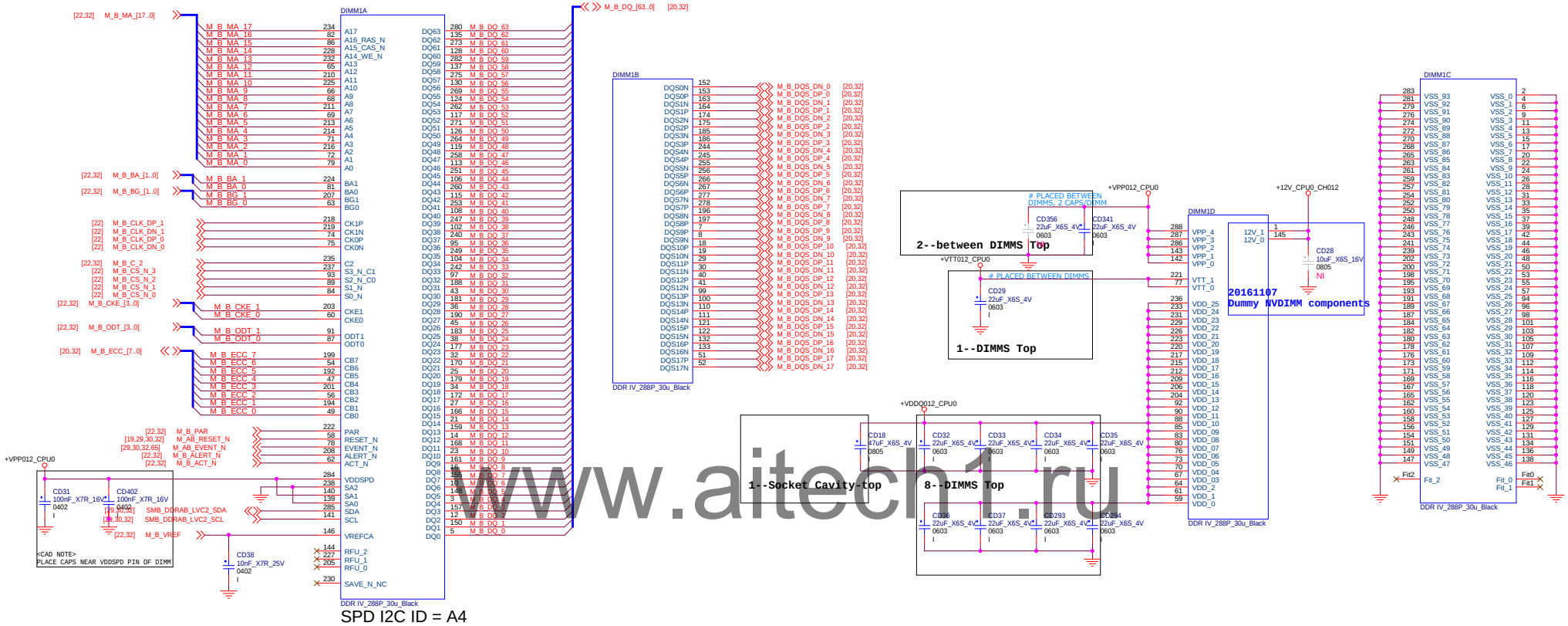
DDR4 DIMM1 CPU0.CHB.D0



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TITLE	DDR4 DIMM1 CPU0.CHB.D0		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	31 of 147

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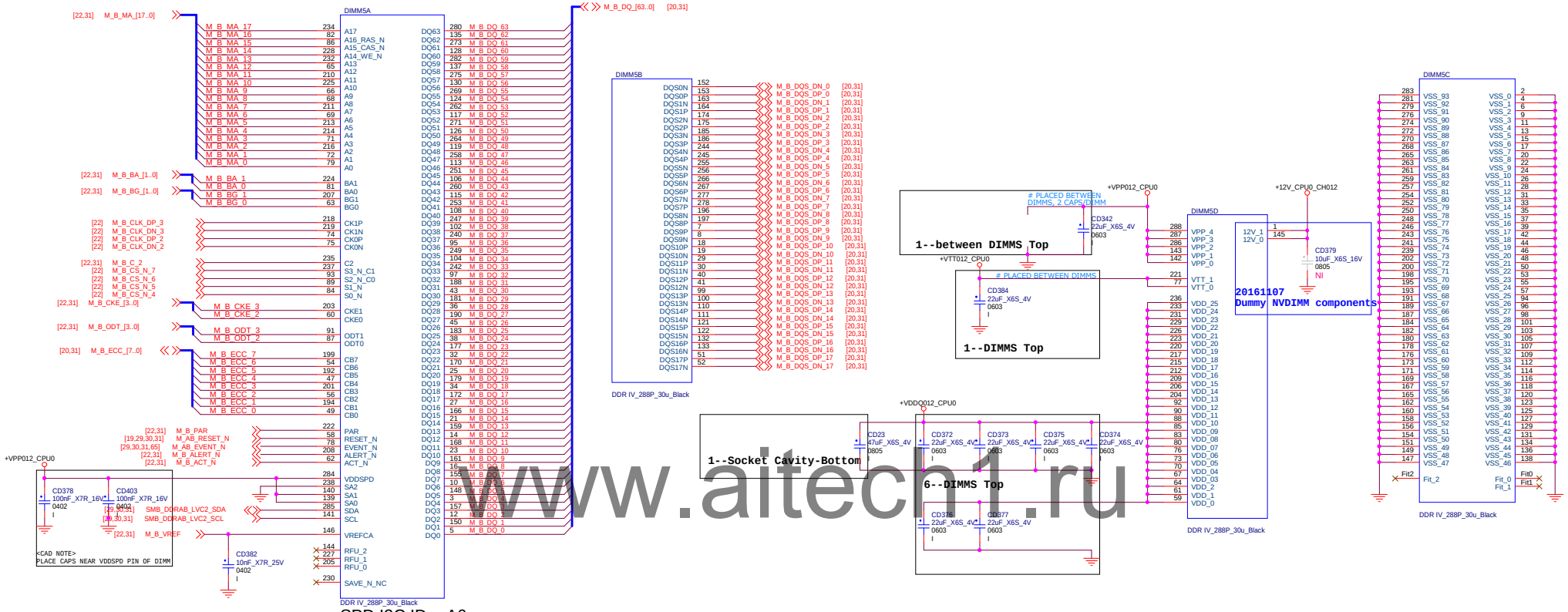
DDR4 DIMM5 CPU0.CHB.D1



SPD I2C ID = A6

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TITLE	DDR4 DIMM5 CPU0.CHB.D1		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	32 of 147

COMPRESSED IMAGE

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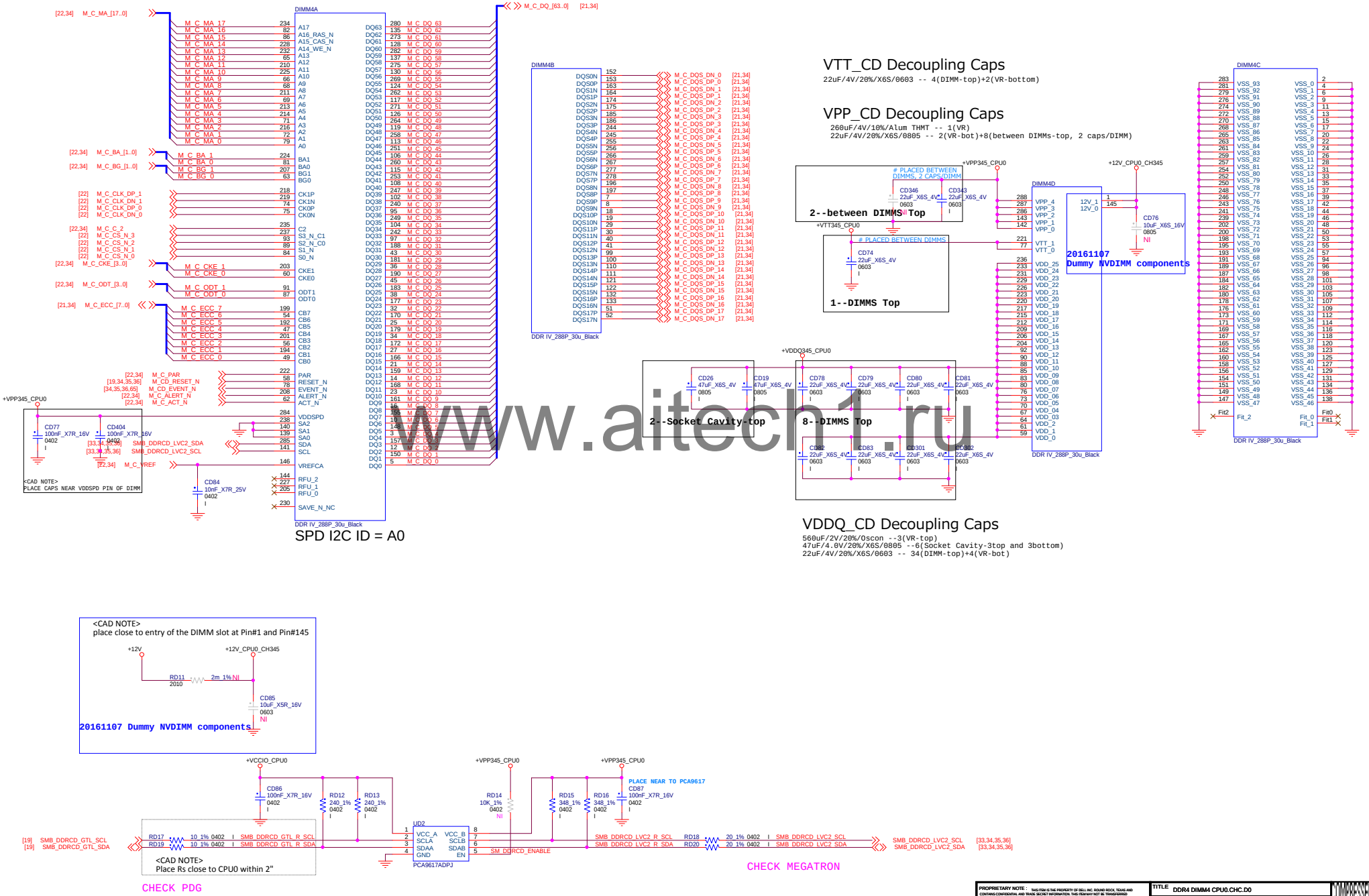

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TITLE	DDR4 DIMM4 CPU0.CHC.D0		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	33 of 147

COMPRESSED IMAGE

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TSOD = 0x38

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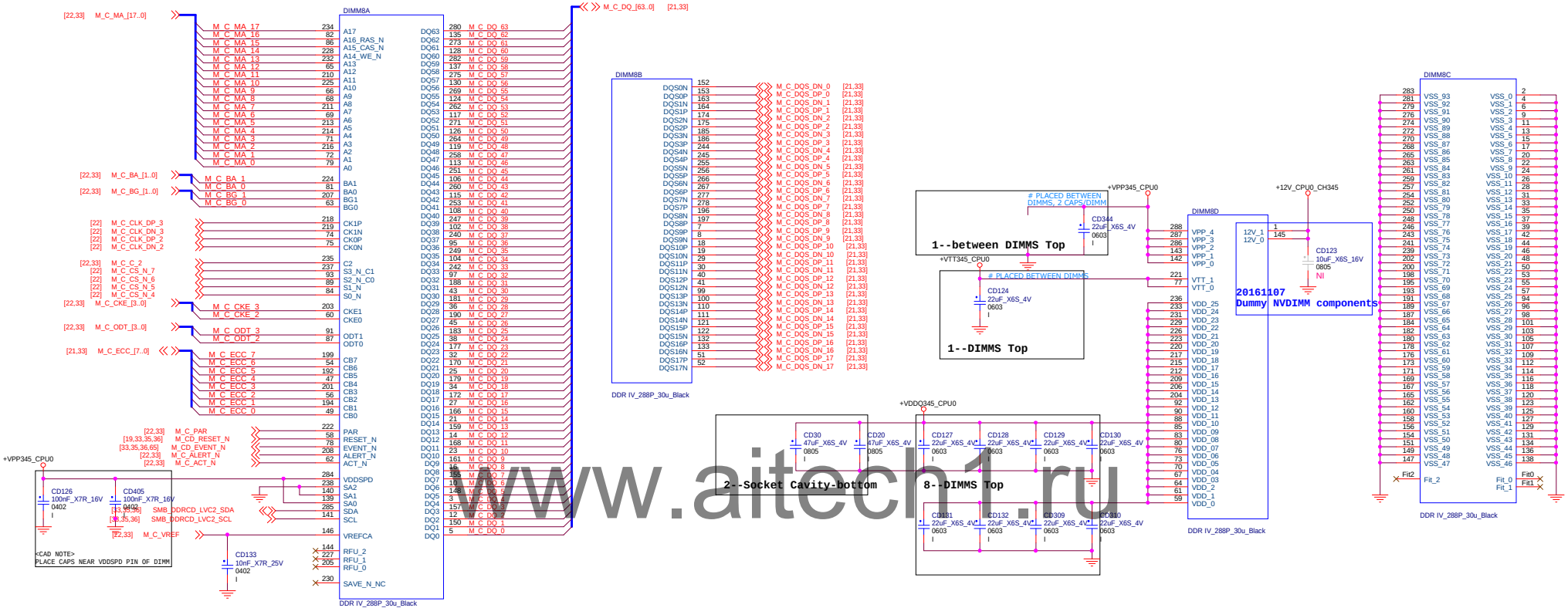

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TITLE	DDR4 DIMM8 CPU0.CHC.D1		
DWG NO.	MATIRA 3	REV.	A00
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COMPRESSED IMAGE

SA[2:0] = 010
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TSOD = 0x34

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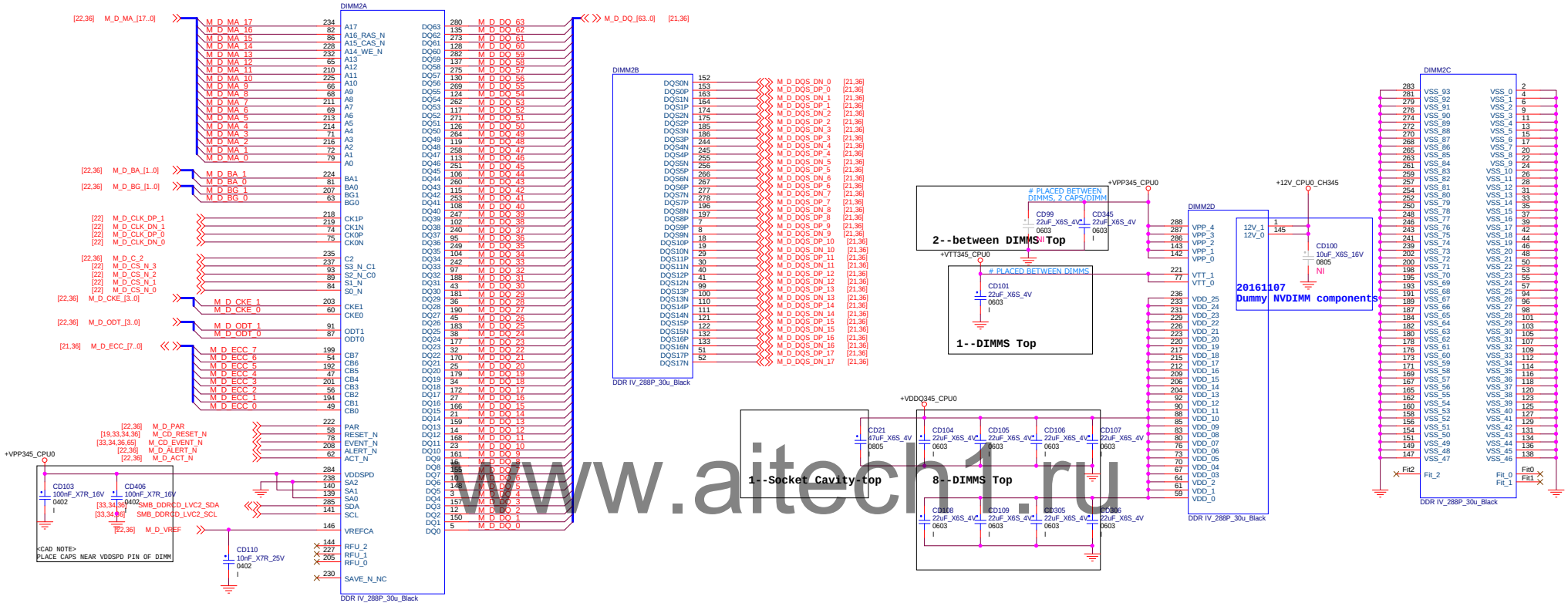

SPD I2C ID = A4

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TITLE	DDR4 DIMM2 CPU0.CHD.D0		
DWG NO.	MATIRA 3	REV.	A00
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COMPRESSED IMAGE

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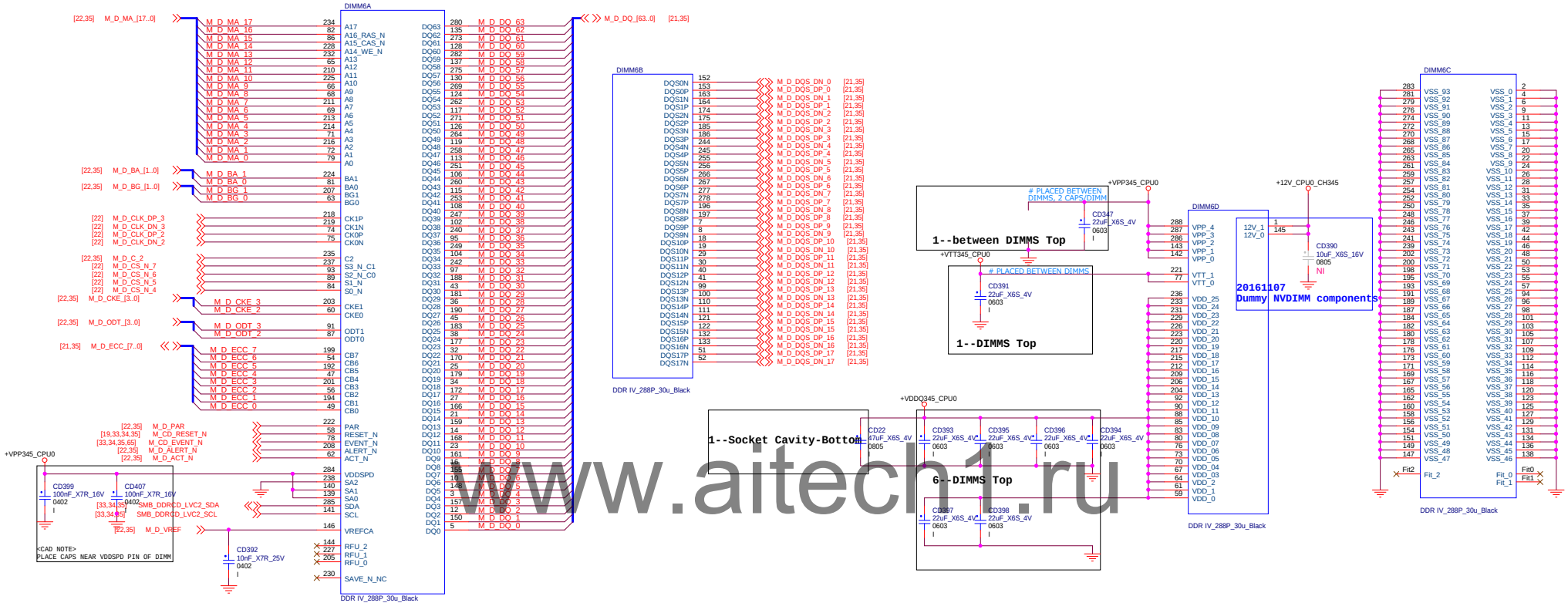

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TITLE	DDR4 DIMM6 CPU0.CHD.D1		
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DWG NO.	MATIRA 3	REV.	A00
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TITLE	BLANK		
DWG NO.	MATIRA 3	REV.	A00
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TITLE	BLANK		
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TITLE	BLANK		
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TITLE	BLANK		
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TITLE	BLANK		
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TITLE	BLANK		
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TITLE	BLANK		
DWG NO.	MATIRA 3	REV.	A00
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DMI

Midbus Footprint

[77]	DMI_CPU0_PCH_TX_C_NB_DP_0	DMI_CPU0_PCH_TX_C_NB_DP_0	CX1	220nF X7R 16V 0402	DMI_CPU0_PCH_TX_NB_DP_0	[23]
[77]	DMI_CPU0_PCH_TX_C_NB_DN_0	DMI_CPU0_PCH_TX_C_NB_DN_0	CX4	220nF X7R 16V 0402	DMI_CPU0_PCH_TX_NB_DN_0	[23]
[77]	DMI_CPU0_PCH_TX_C_NB_DP_1	DMI_CPU0_PCH_TX_C_NB_DP_1	CX6	220nF X7R 16V 0402	DMI_CPU0_PCH_TX_NB_DP_1	[23]
[77]	DMI_CPU0_PCH_TX_C_NB_DN_1	DMI_CPU0_PCH_TX_C_NB_DN_1	CX9	220nF X7R 16V 0402	DMI_CPU0_PCH_TX_NB_DN_1	[23]
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[77]	DMI_CPU0_PCH_TX_C_NB_DN_2	DMI_CPU0_PCH_TX_C_NB_DN_2	CX14	220nF X7R 16V 0402	DMI_CPU0_PCH_TX_NB_DN_2	[23]
[77]	DMI_CPU0_PCH_TX_C_NB_DP_3	DMI_CPU0_PCH_TX_C_NB_DP_3	CX16	220nF X7R 16V 0402	DMI_CPU0_PCH_TX_NB_DP_3	[23]
[77]	DMI_CPU0_PCH_TX_C_NB_DN_3	DMI_CPU0_PCH_TX_C_NB_DN_3	CX19	220nF X7R 16V 0402	DMI_CPU0_PCH_TX_NB_DN_3	[23]
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[77]	DMI_CPU0_PCH_RX_SB_DN_0		CX28	220nF X7R 16V 0402	DMI_CPU0_PCH_RX_C_SB_DN_0	[23]
[77]	DMI_CPU0_PCH_RX_SB_DP_1		CX31	220nF X7R 16V 0402	DMI_CPU0_PCH_RX_C_SB_DP_1	[23]
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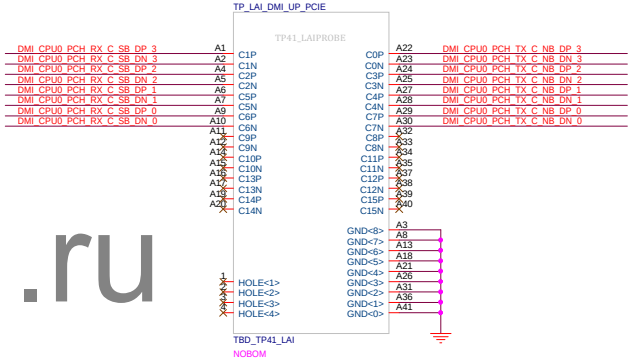
[77]	DMI_CPU0_PCH_RX_SB_DN_2		CX38	220nF X7R 16V 0402	DMI_CPU0_PCH_RX_C_SB_DN_2	[23]
[77]	DMI_CPU0_PCH_RX_SB_DP_3		CX41	220nF X7R 16V 0402	DMI_CPU0_PCH_RX_C_SB_DP_3	[23]
[77]	DMI_CPU0_PCH_RX_SB_DN_3		CX43	220nF X7R 16V 0402	DMI_CPU0_PCH_RX_C_SB_DN_3	[23]

DMI/UPLINK LAI Connector



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TITLE	DMI_LAI/UPLINK		
DWG NO.	MATIRA 3	REV.	A00
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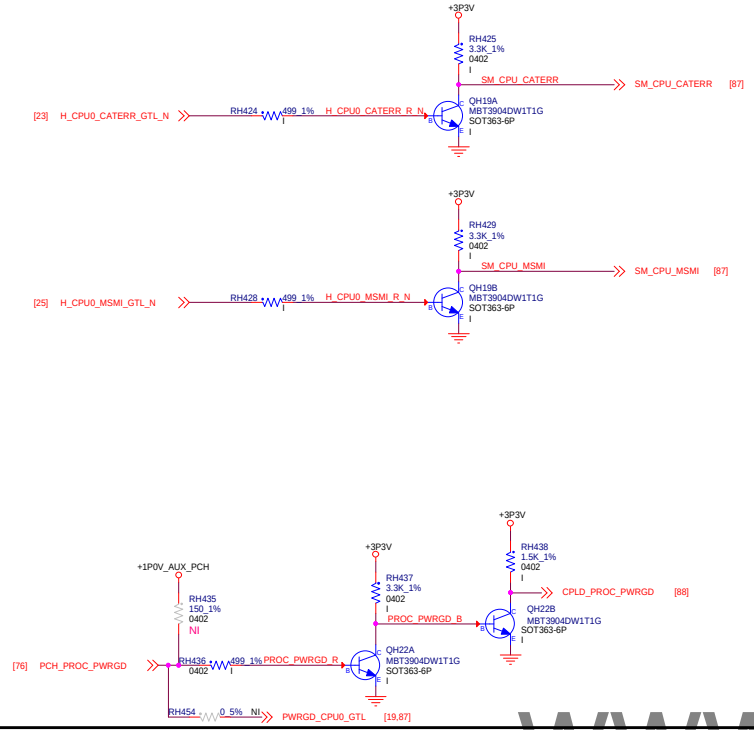
CRTERR / MSMI / EAR / CPU PG



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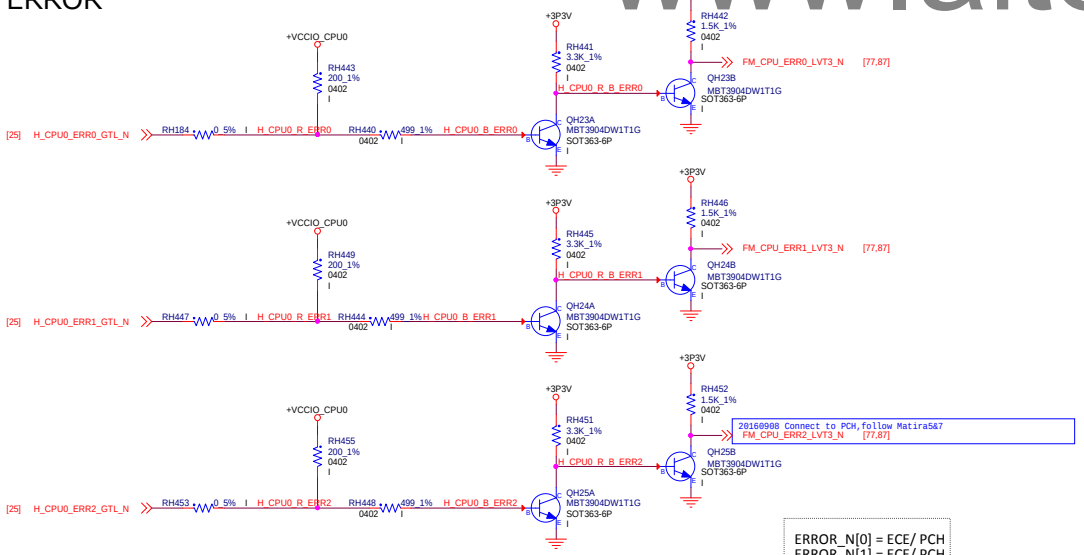

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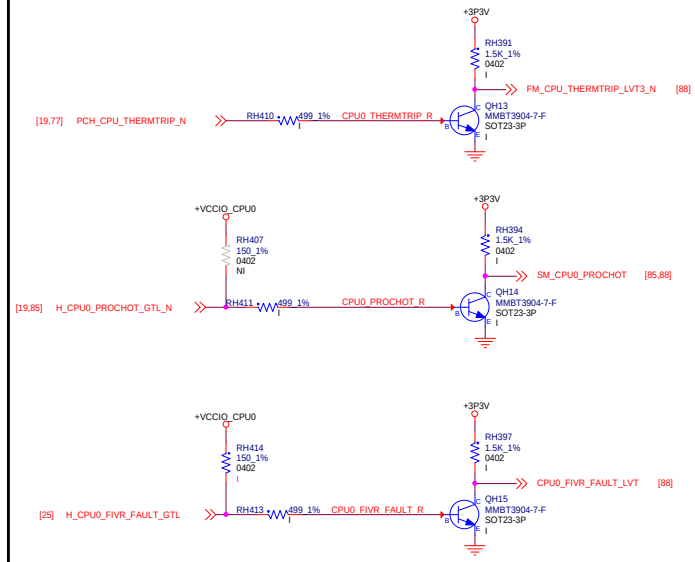

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TITLE	CPU Common Logic - 1OF2		
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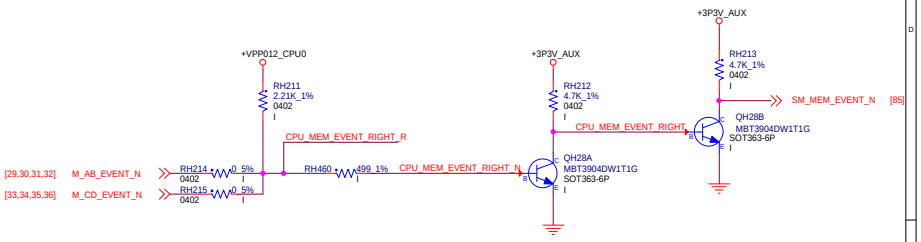
COMPRESSED IMAGE

HOT

CPU PG / CPU RST

MEM PG

MEM EVENT



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TITLE	CPU Common Logic - 2OF2		
DWG NO.	MATIRA 3	REV.	A00
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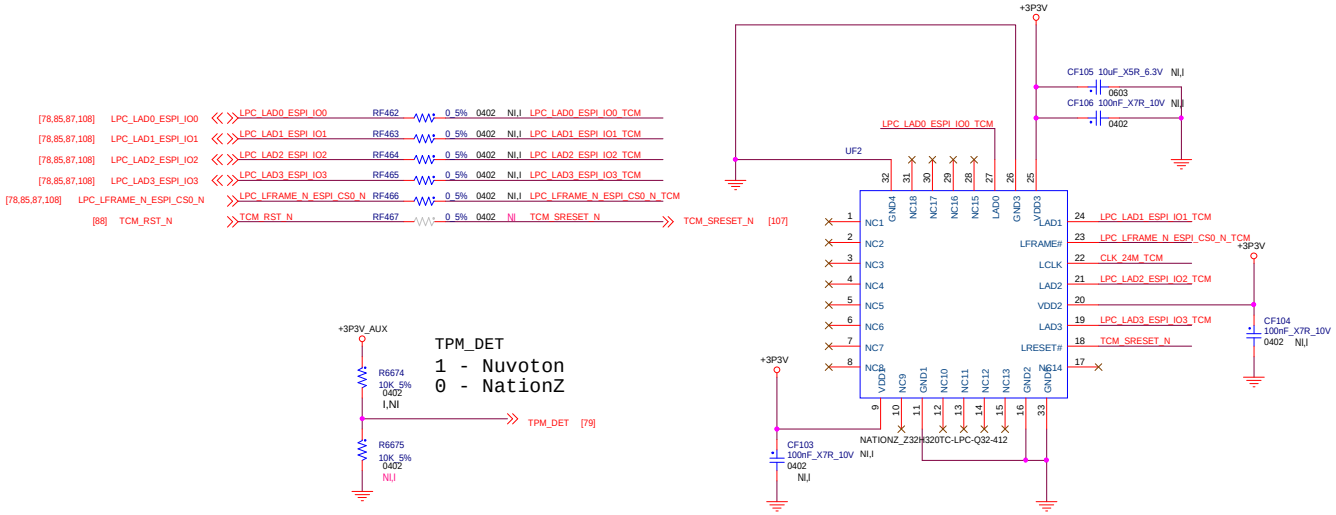
UNCLASSIFIED IMAGE



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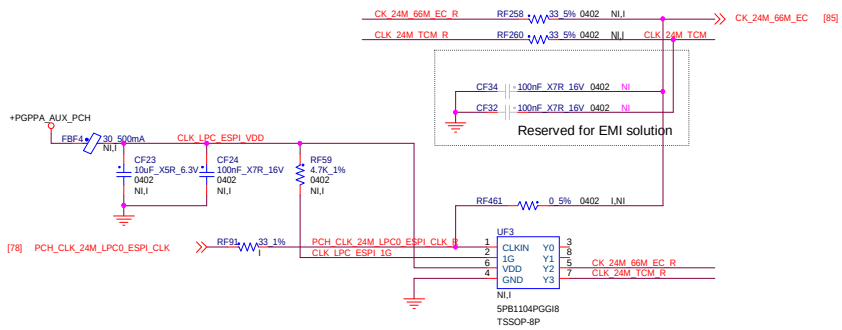
LPC CLOCK BUFFER



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TITLE	Clock Buffer/TPM		
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DWG NO: MATRIX 3		REV: A00	
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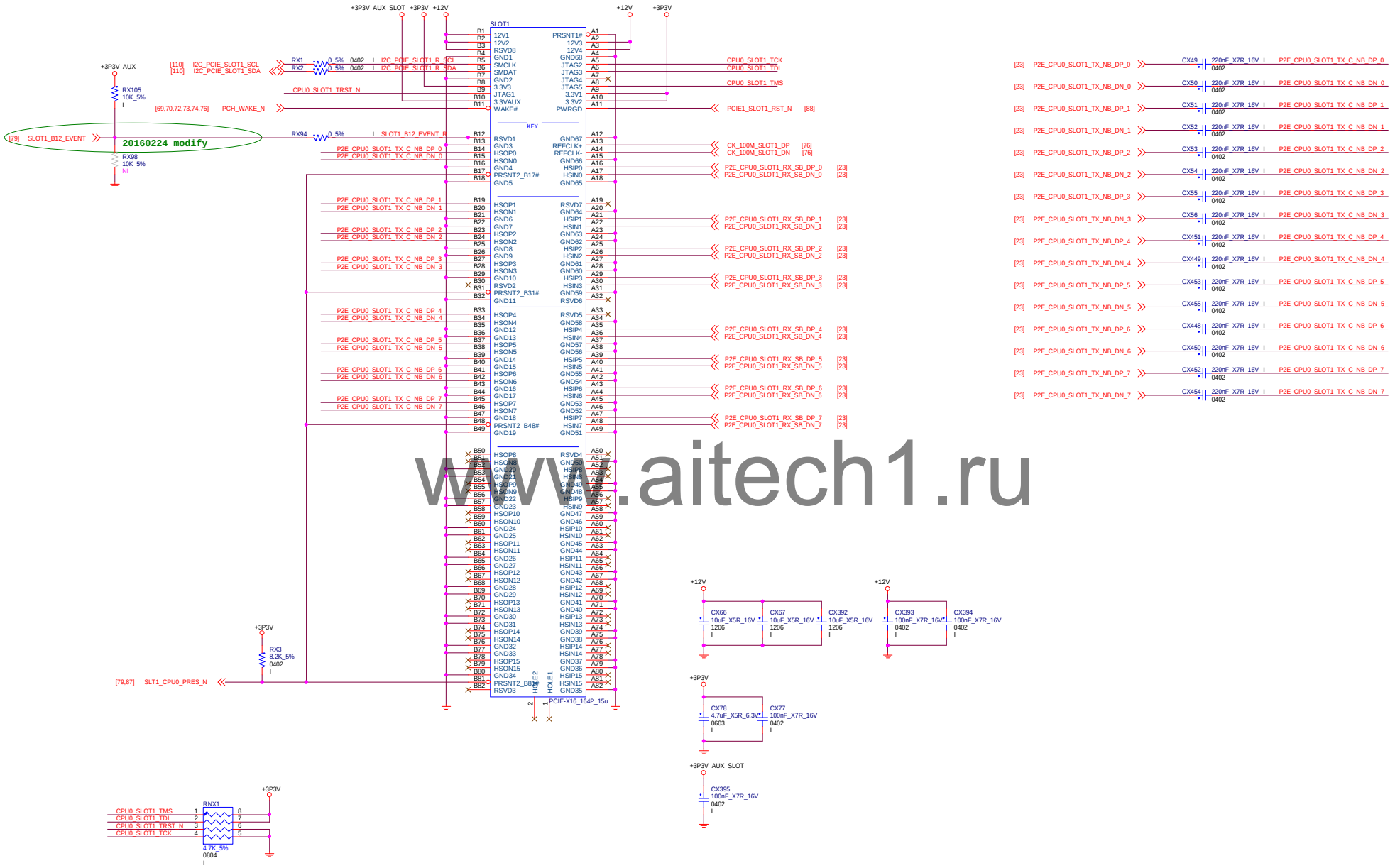
PCIE x16 SLOT1 (CPU0 WIRED 8x GEN3)



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TITLE	PCIE G3 X16-Slot1_CPU0_8x
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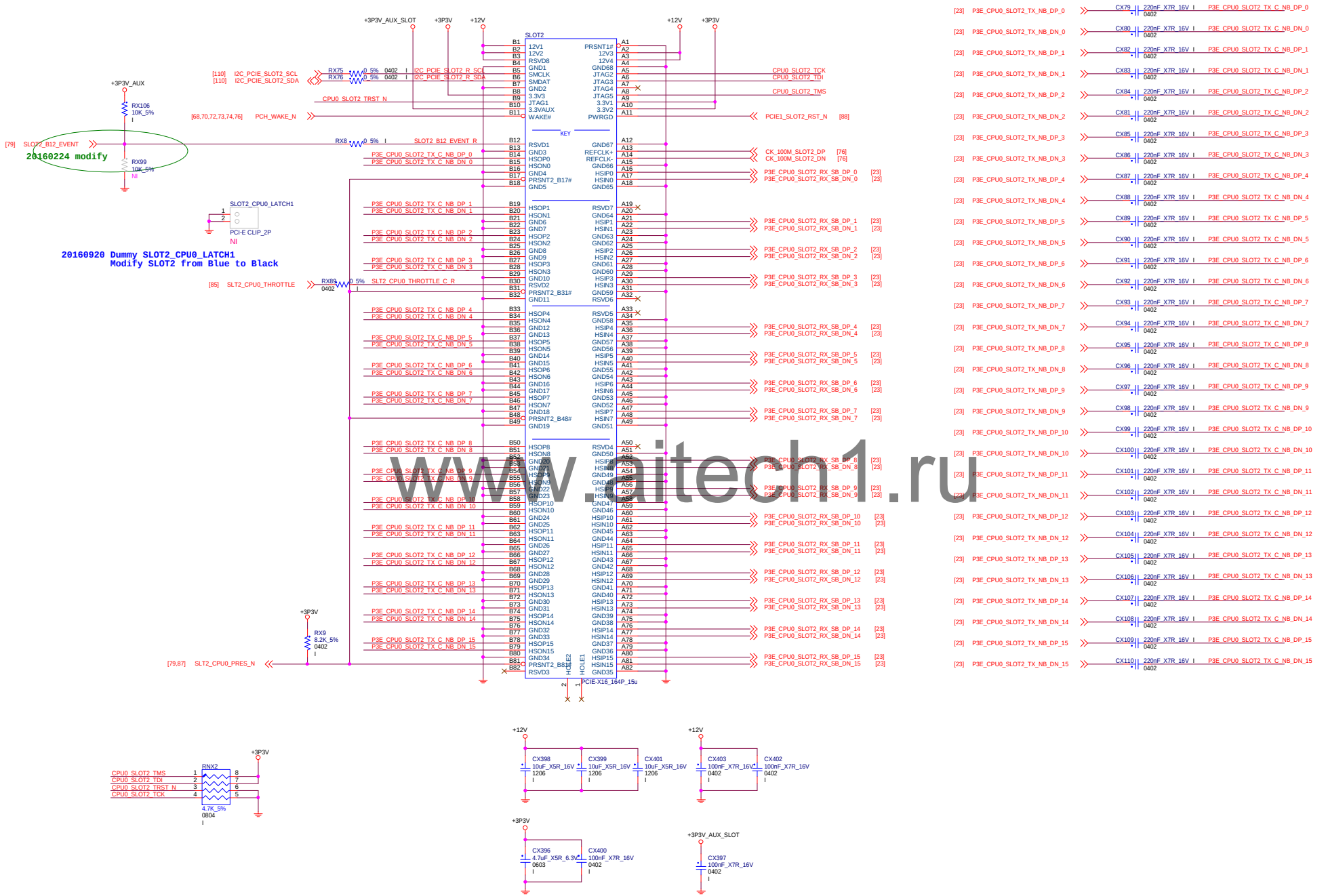
PCIE x16 SLOT2 (CPU0 WIRED 16X GEN3)



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TITLE	PCIE G3 X16-Slot2_CPU0		
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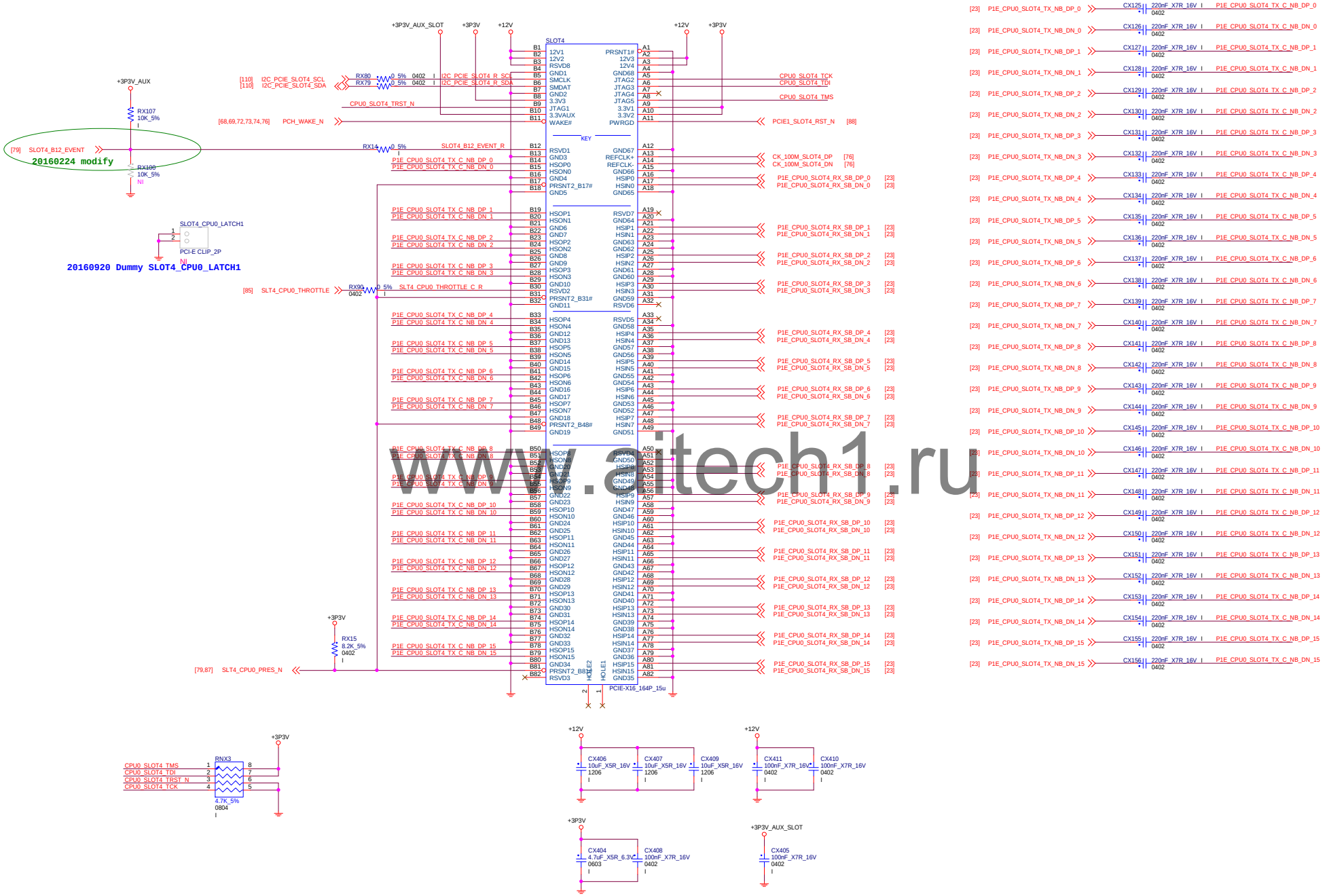
PCIE x16 SLOT4 (CPU0 WIRED 16X GEN3)



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TITLE	PCIE G3 X16-Slot4_CPU0		
DWG NO.	MATIRA 3	REV.	A00
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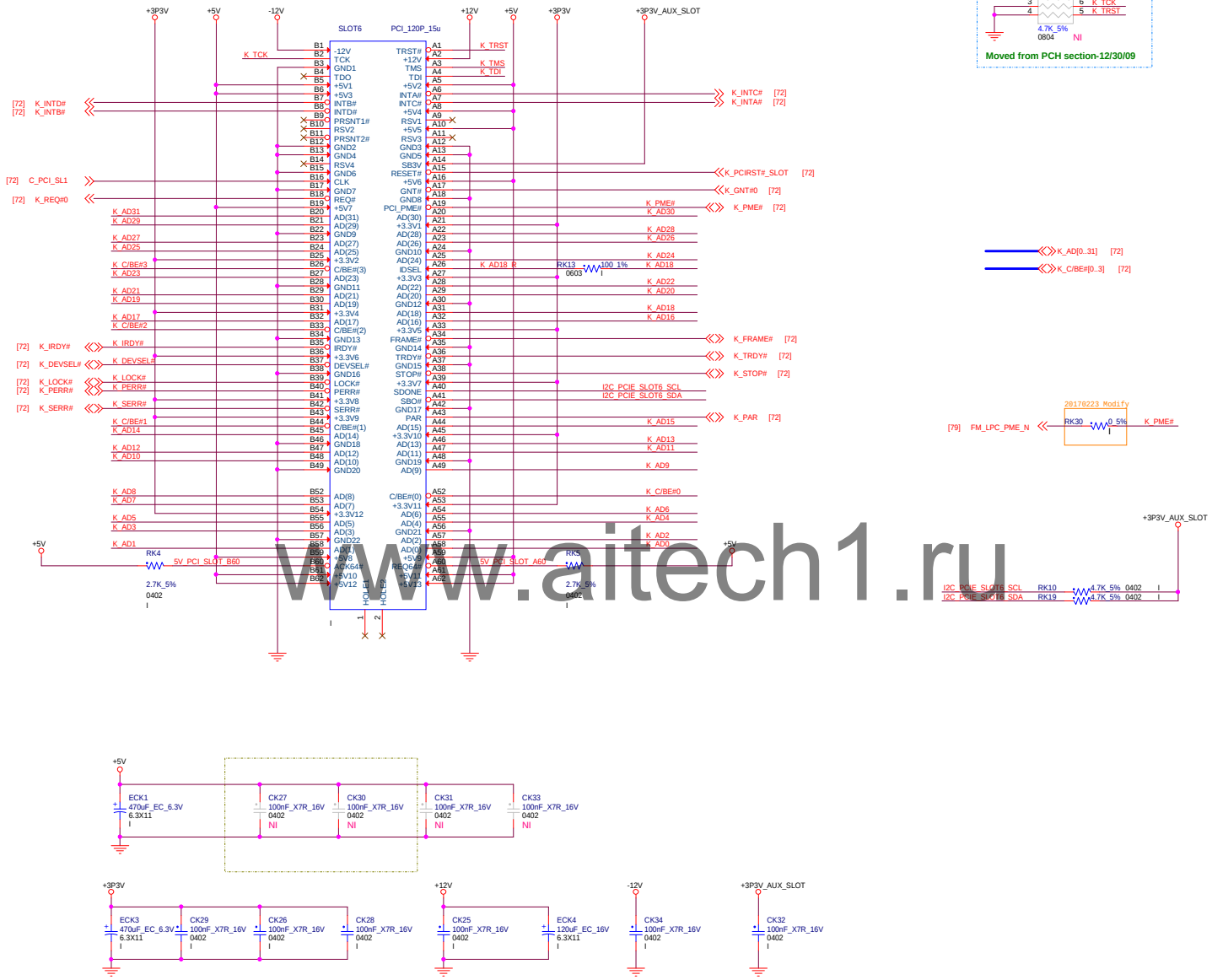

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TITLE	PCI-Slot6		
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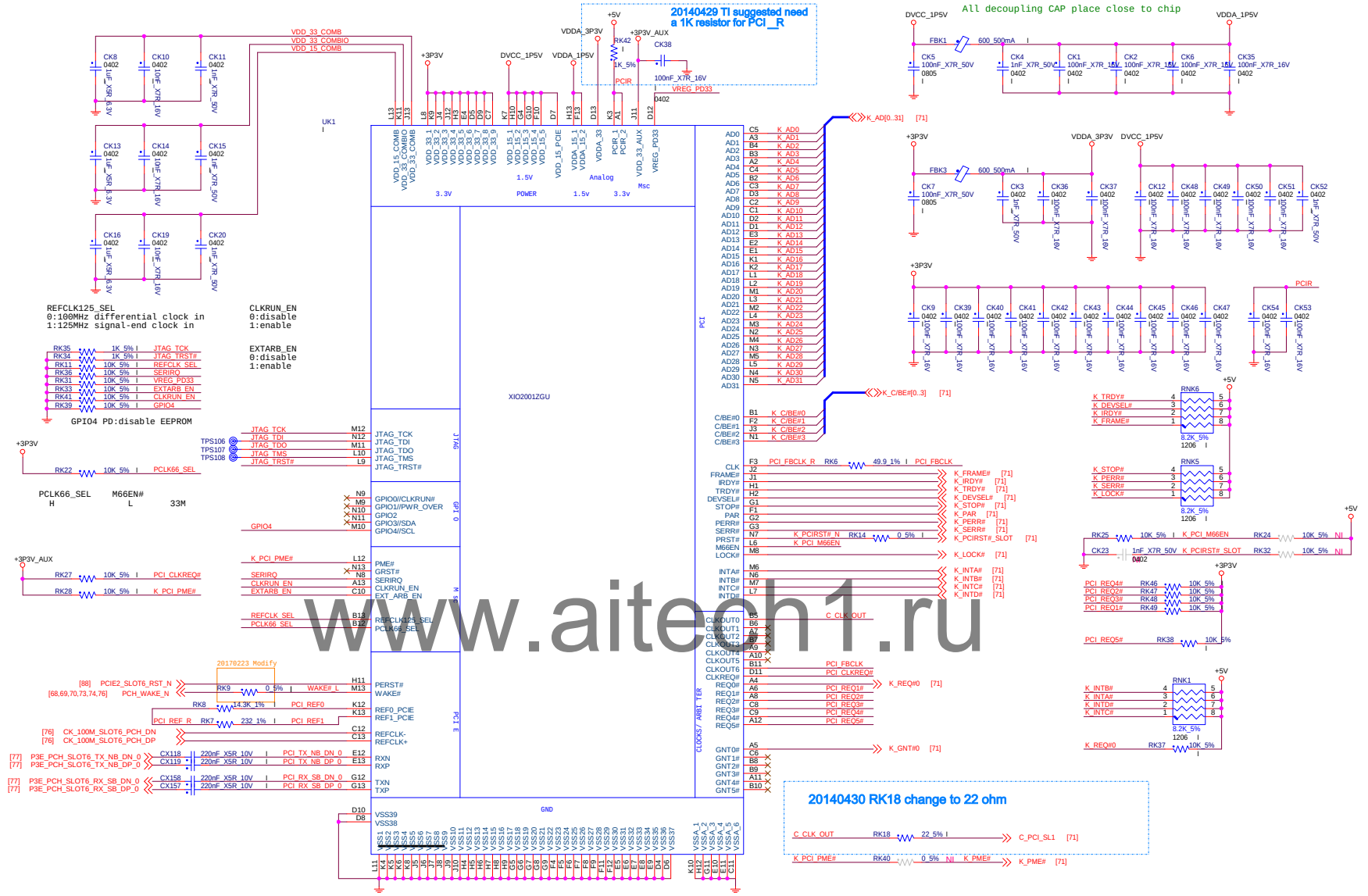
COMPRESSED IMAGE



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TITLE	PCIe to PCI_PCH_1x
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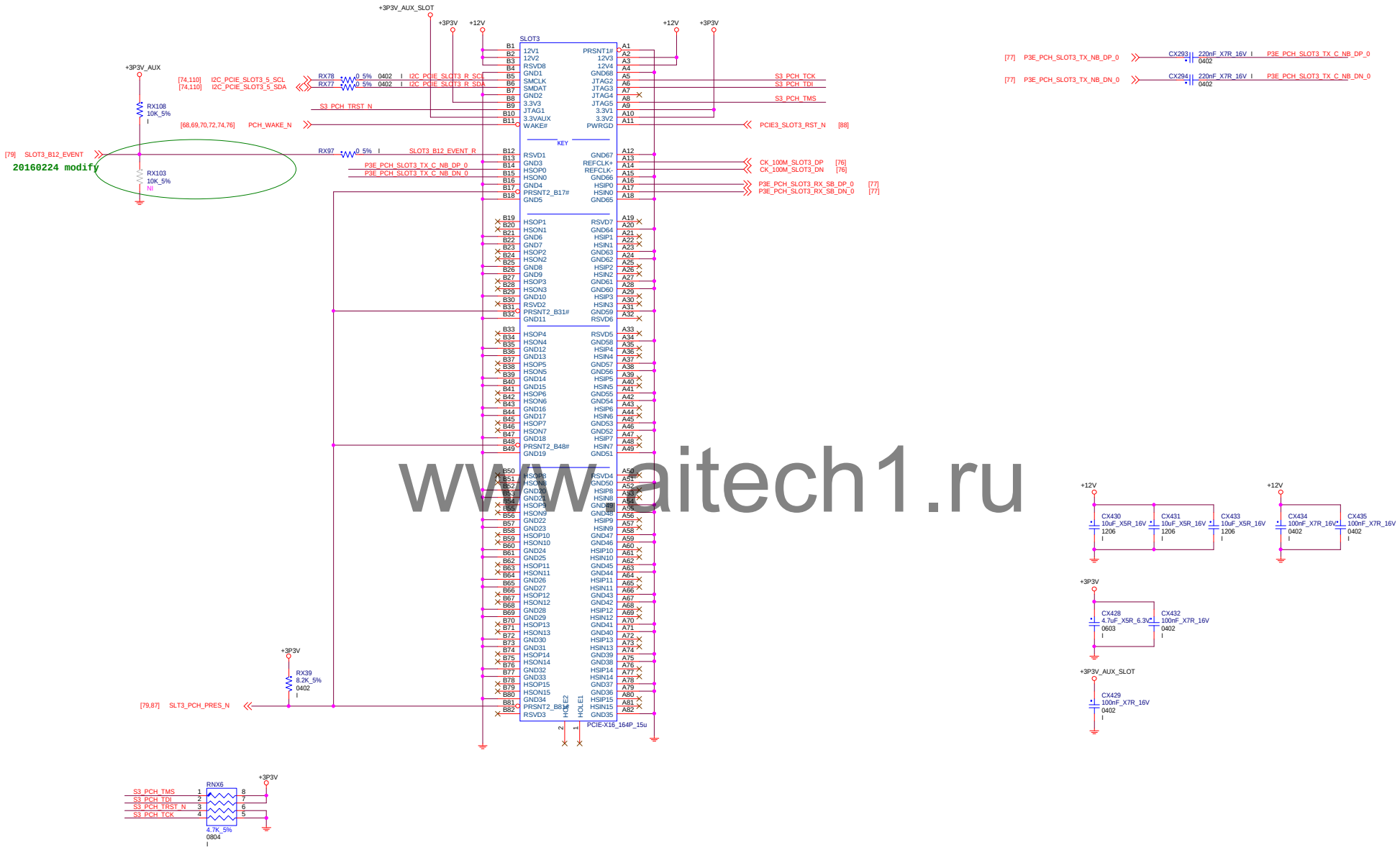
COMPRESSED IMAGE

PCIE x16 SLOT3 (PCH WIRED 1X GEN3)



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TITLE	PCIE G3 X16-Slot3_PCH_1x		
DWG NO.	MATIRA 3	REV.	A00
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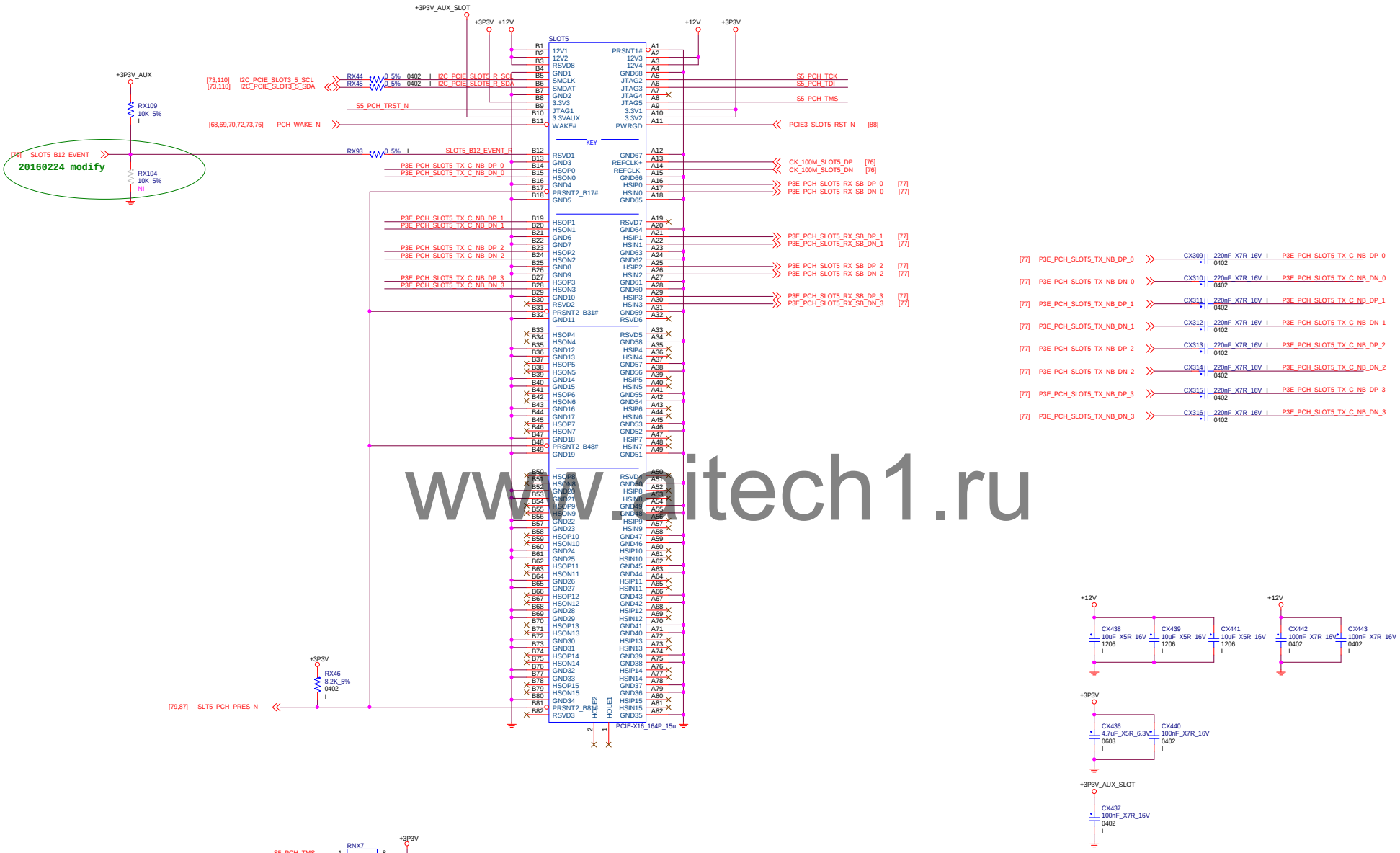
PCIE x16 SLOT5 (PCH WIRED 4X GEN3)



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	DWG NO. MATIRA 3	REV. A00	
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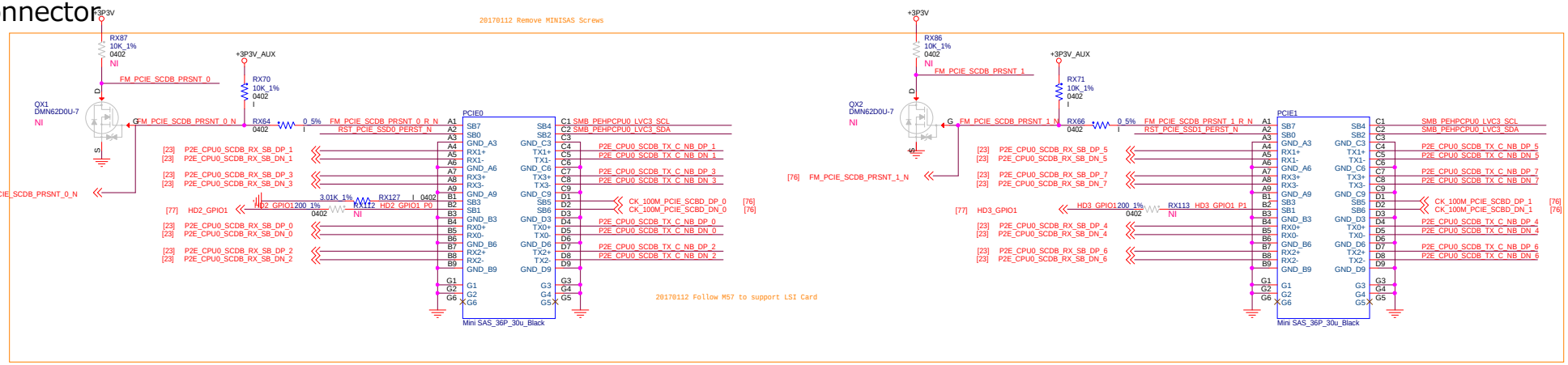
COMPRESSED IMAGE

CPU PCIE Storage Connector



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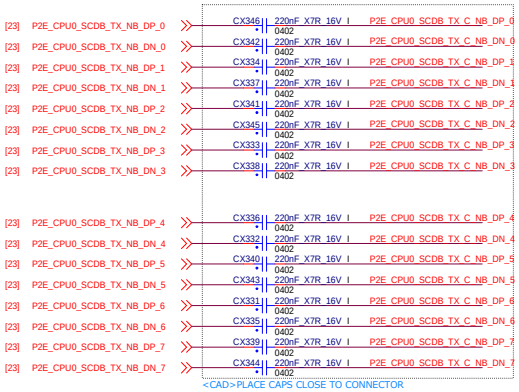

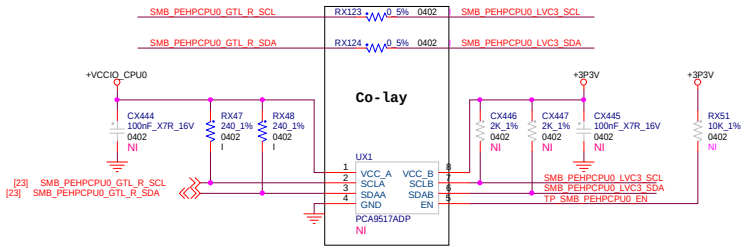

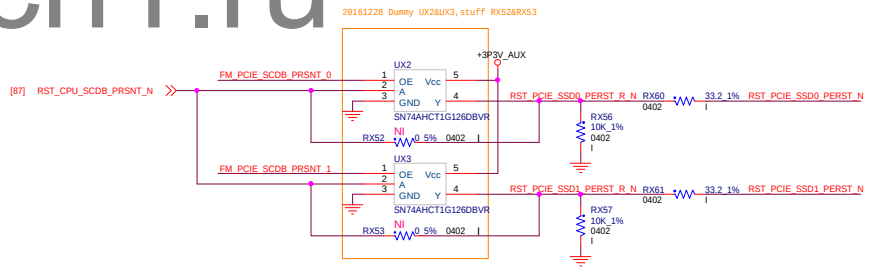

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TITLE	PCIE Storage Connector		
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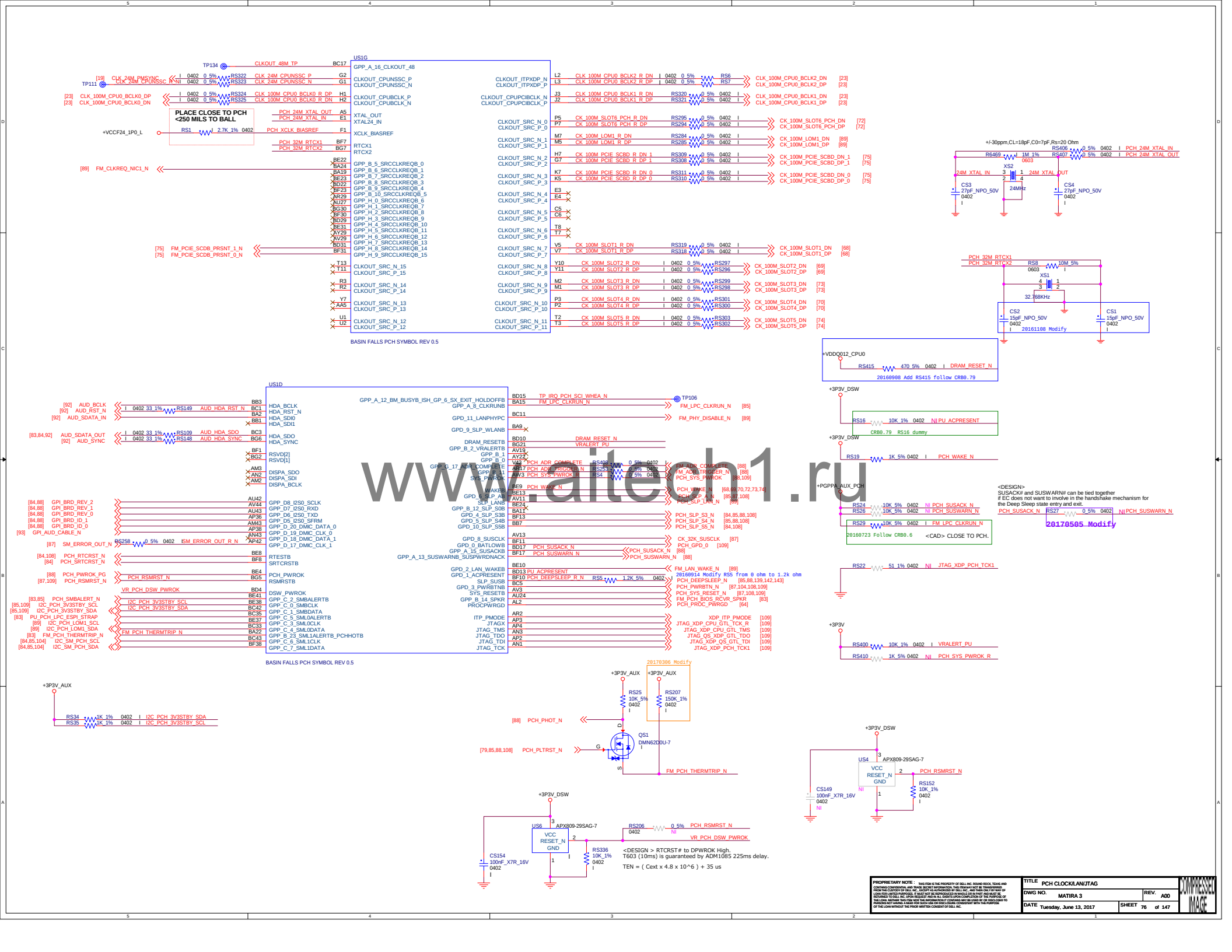
J-COMPRESSED IMAGE



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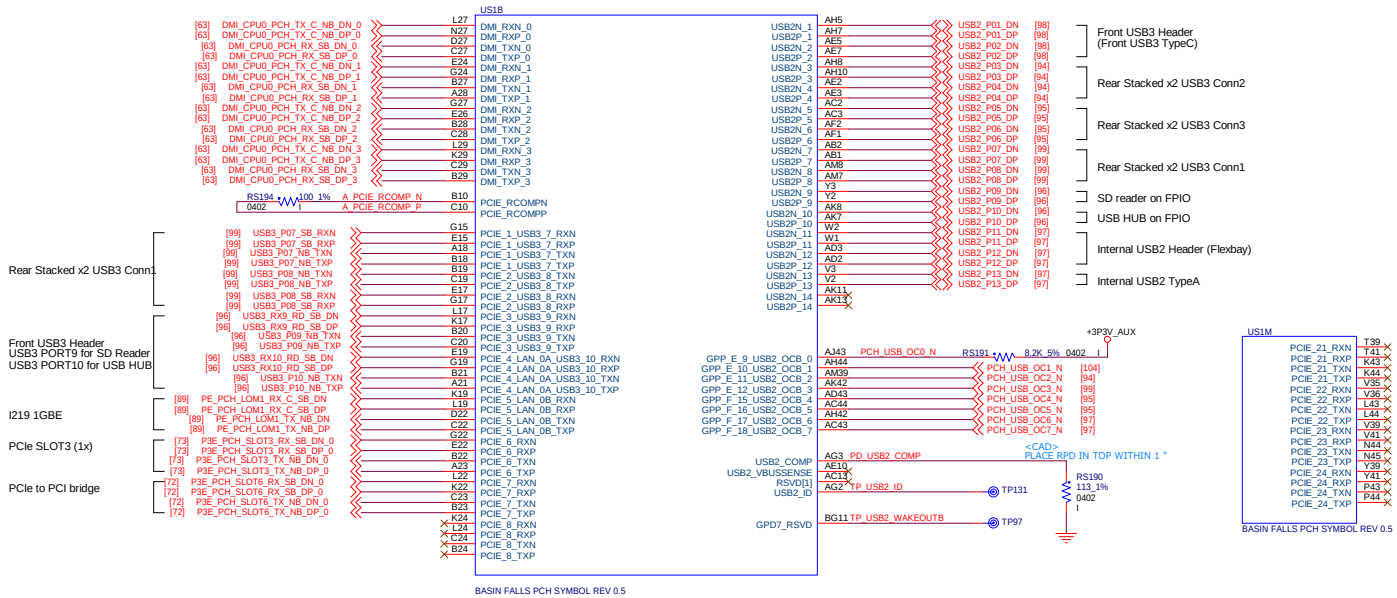


USB Port Mapping Table

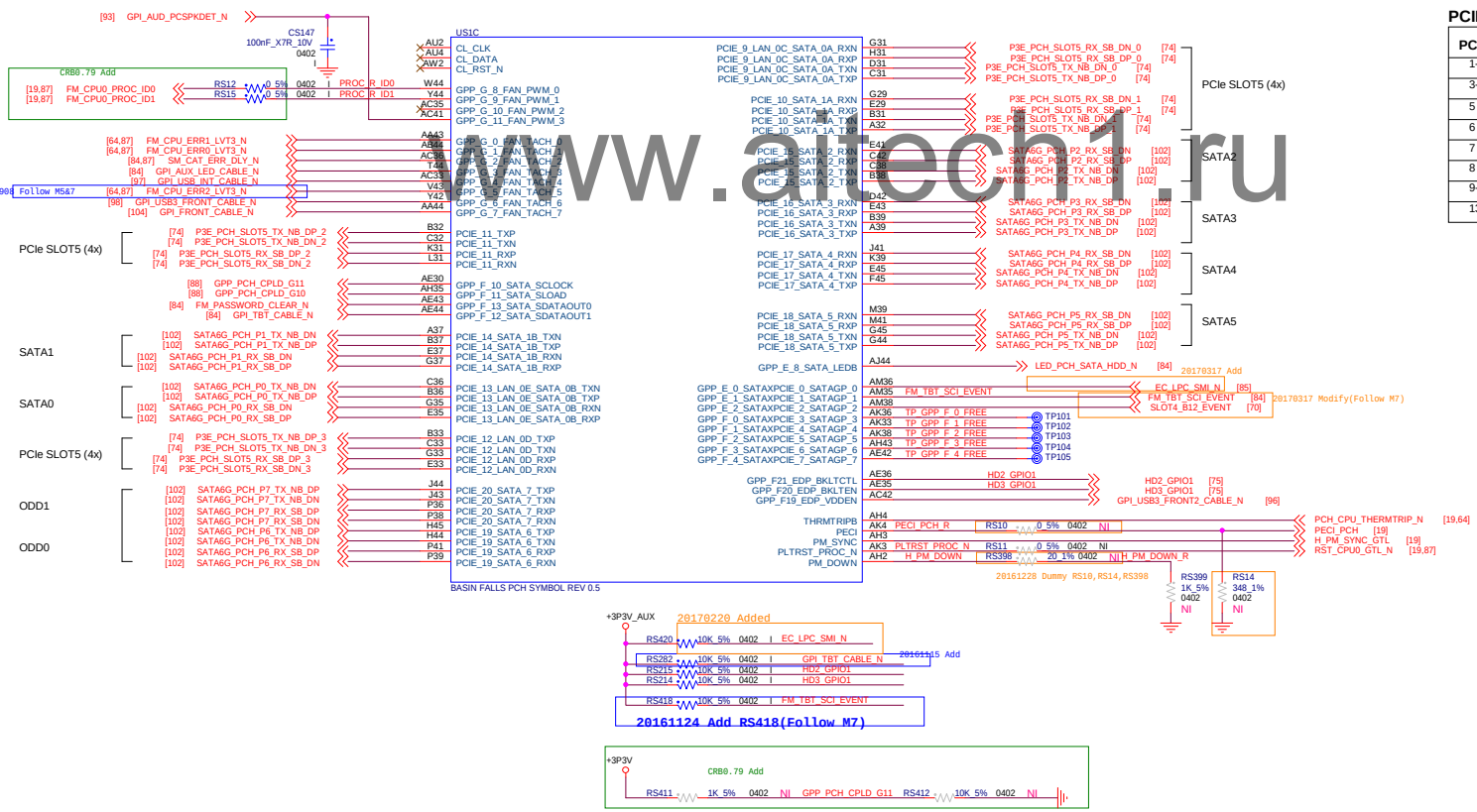
USB3	USB2	OC#	Location
1-2	1-2	1	Front USB3 Header(For TypeC)
3-4	3-4	2	Rear Stacked x2 USB3 Conn2
5-6	5-6	4-5	Rear Stacked x2 USB3 Conn3
7-8	7-8	3	Rear Stacked x2 USB3 Conn1
9-10	9-10	N/A	Internal USB3 Header(SD+HUB)
	11-12	7	Internal USB2 Header (Flexbay)
	13	6	Internal USB2

SATA Port Mapping Table

SATA3	SSATA3	Location
0-5	Y	SATA0-SATA5
6-7	Y	ODD0-ODD1

PCIE Port Mapping Table

PCIe3	Function	Location
1-2		Rear Stacked x2 USB3 Conn1
3-4		Internal USB3 Header(SD+HUB)
5	Y	I219 1GBE
6	Y	PCIe SLOT 3 (1x)
7	Y	PCIe-PCI Bridge
8		NC
9-12	Y	PCIe SLOT5 (4x)
13-20		SATA0-SATA5 ODD0-ODD1



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TITLE	PCH USB/PCIE/DMI		
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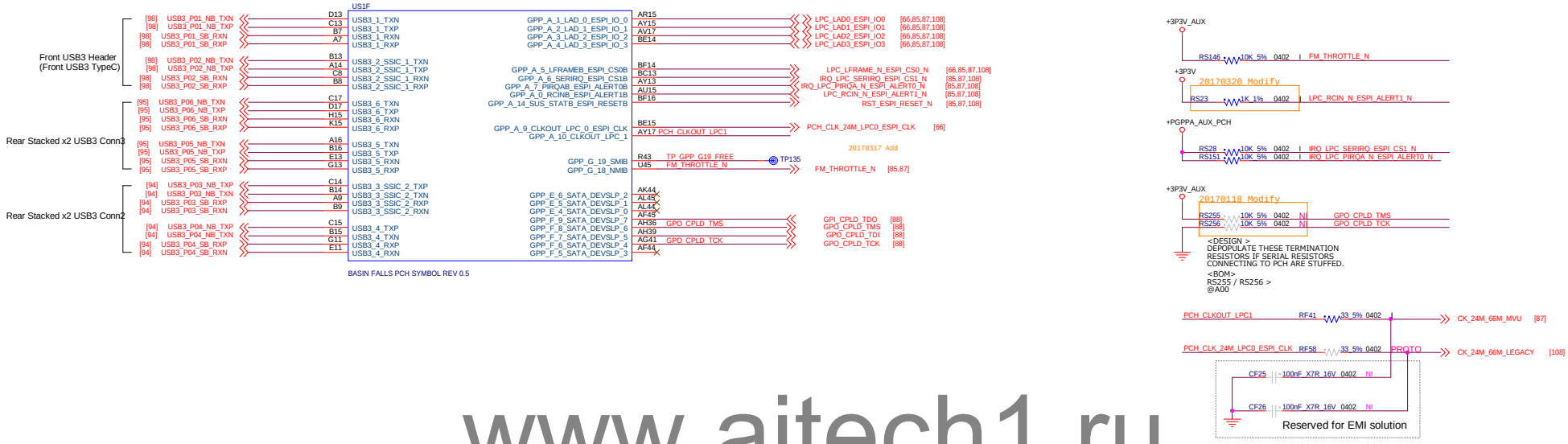

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TITLE	PCH USB3		
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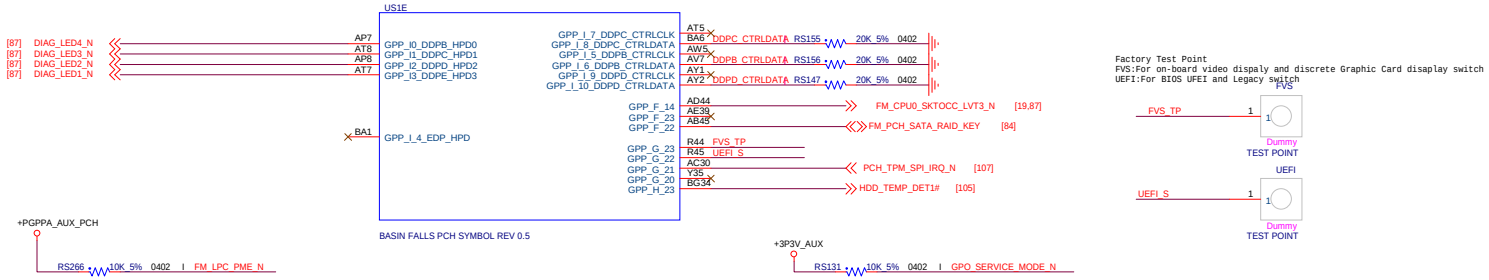
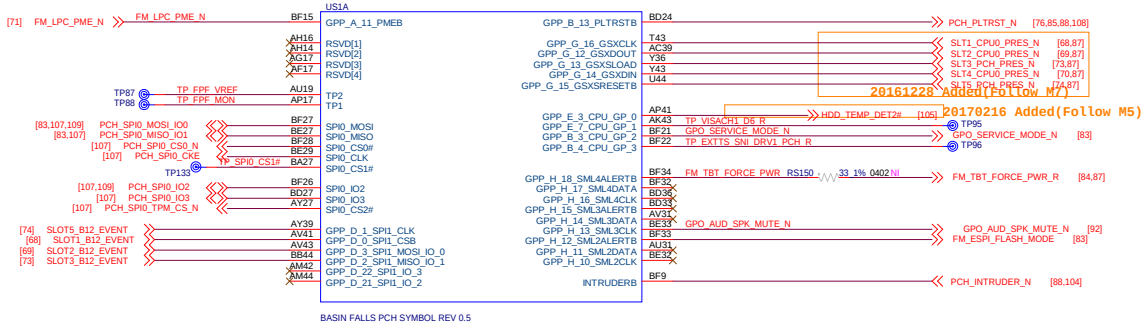
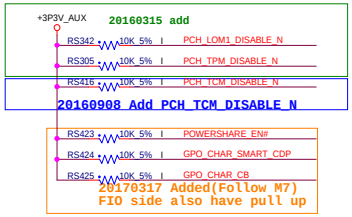
COMPRESSED IMAGE







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TITLE	PCH GPIO		
DWG NO.	MATIRA 3	REV.	A00
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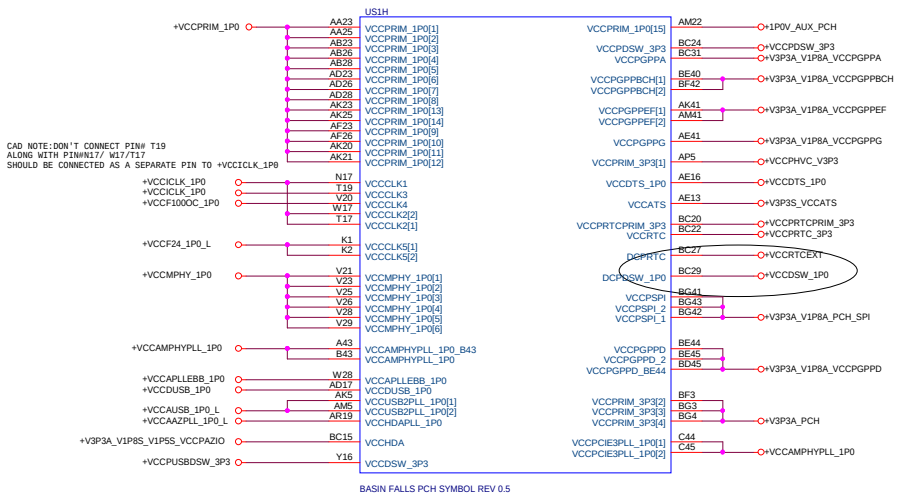
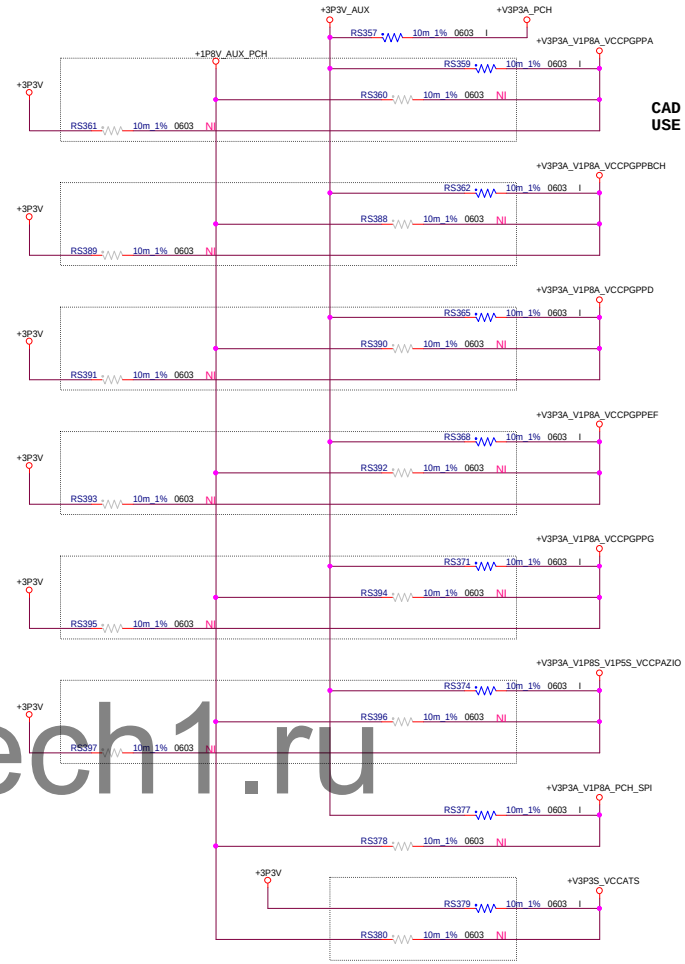
COMPRESSED IMAGE

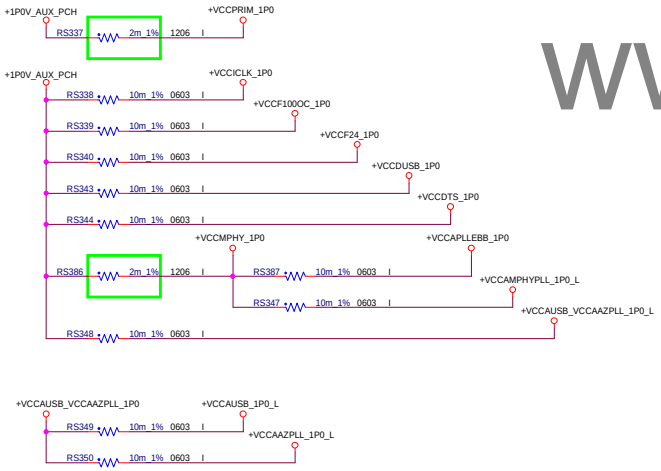


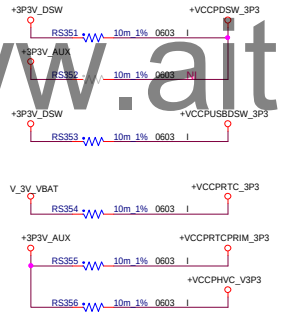
BASIN FALLS PCH SYMBOL REV 0.5

CAD NOTE:
USE 3-PAD SHARING



+V1P05A VR HAS TO BE TUNED TO 1.0V





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TITLE	PCH Power - 1OF2		
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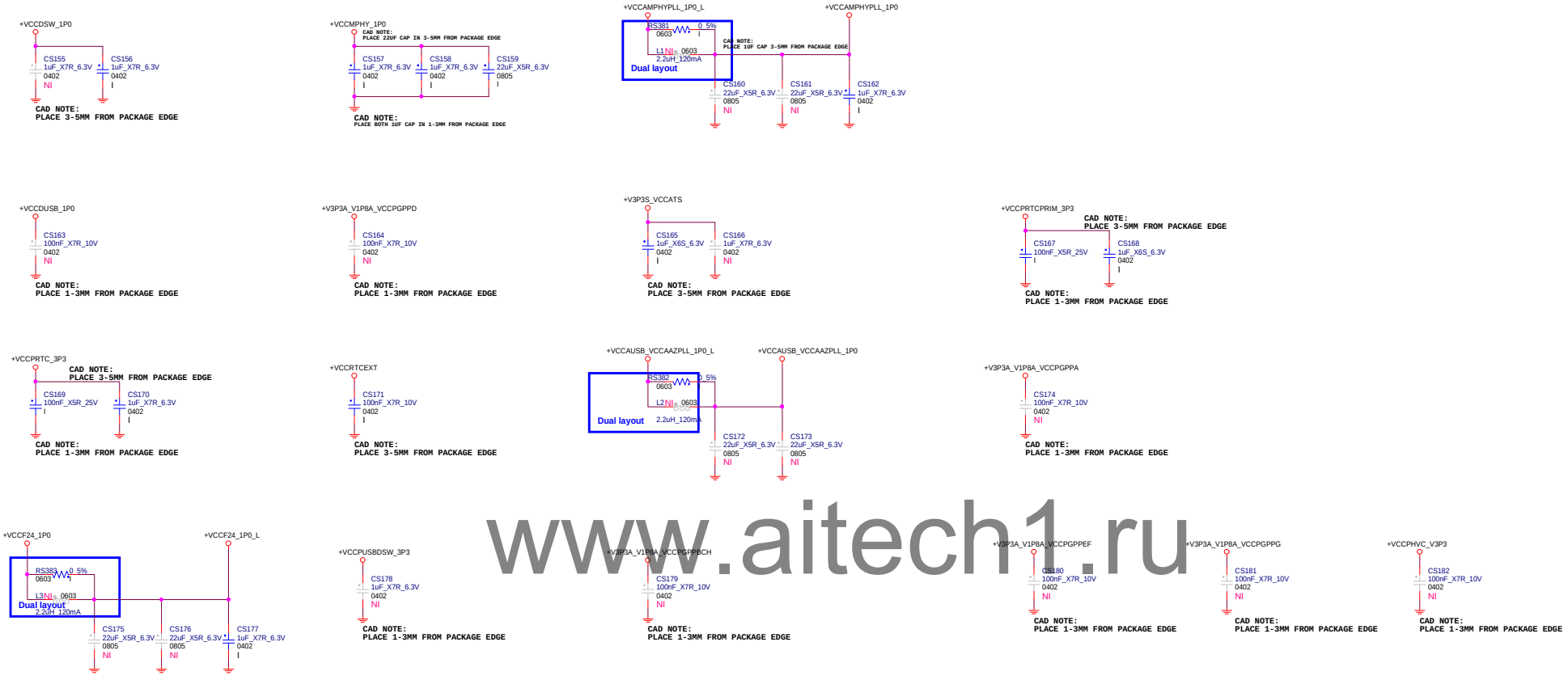

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TITLE	PCH Power - 2OF2		
DWG NO.	MATIRA 3	REV.	A00
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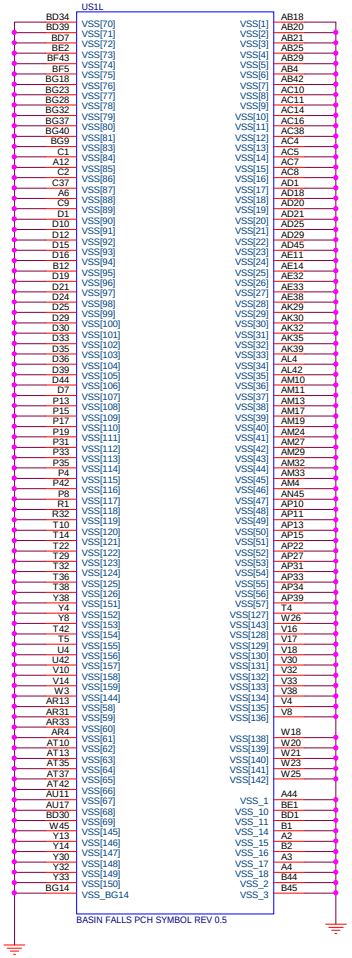
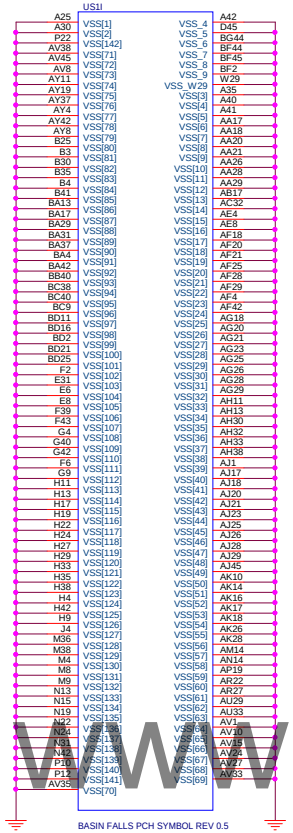
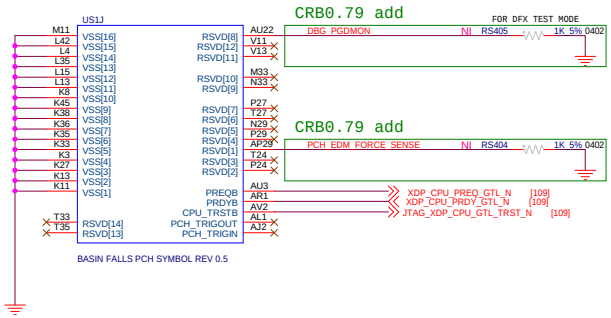
J-IMPRESSED IMAGE







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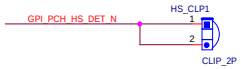
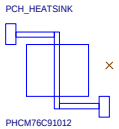
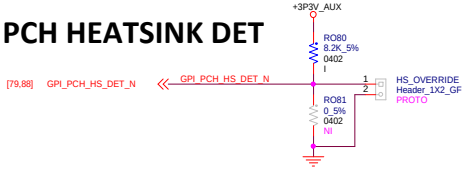




PCH HEATSINK DET



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TITLE	PCH Ground
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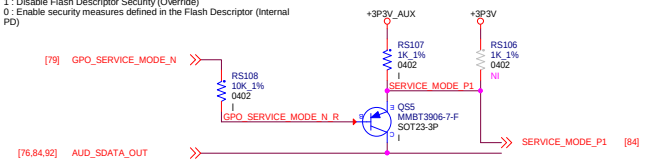
COMPRESSED IMAGE

SERVICE MODE JUMPER

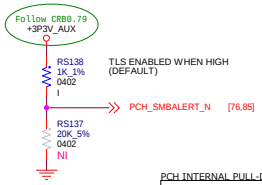
(ME FW Override Jumper)
1 : Disable Flash Descriptor Security (Override)
0 : Enable security measures defined in the Flash Descriptor (Internal PD)



FLASH SECURITY OVERRIDE
PCH INTERNAL PULL-DOWN.

1 > FLASH SECURITY OVERRIDE ENABLE
0 >FLASH SECURITY OVERRYDE DISABLE (DEFAULT)

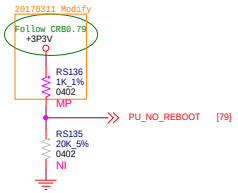
TLS CONFIDENTIALITY



PCH INTERNAL PULL-DOWN.

1 > TLS ENABLED
0 >TLS DISABLE

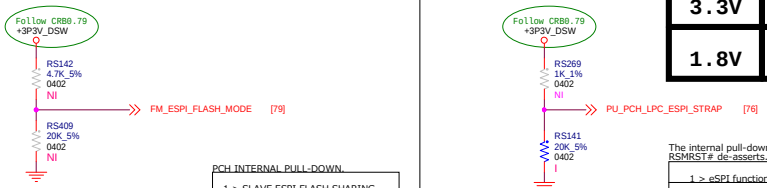
NO REBOOT STRAP



PCH INTERNAL PULL-DOWN.

1 > Enable ¡§No Reboot¡¨ mode. *
0 > Disable ¡§No Reboot¡¨ mode.£¨DefaultE©

ESPI FLASH SHARING MODE

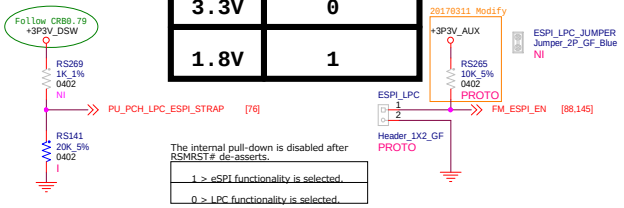


PCH INTERNAL PULL-DOWN.

1 > SLAVE ESPI FLASH SHARING
0 > MASTER ESPI FLASH SHARING (DEFAULT)

ESPI OR LPC

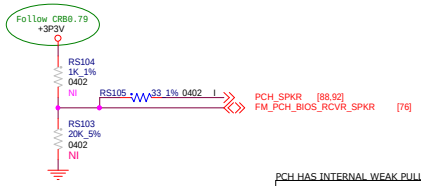
GPPA	FM_ESPI_EN
3.3V	0
1.8V	1



The internal pull-down is disabled after RSMRST# de-asserts.

1 > eSPI functionality is selected.
0 > LPC functionality is selected.

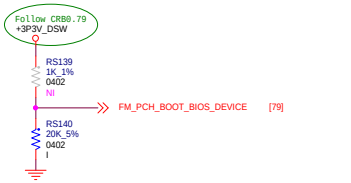
TOP SWAP MODE STRAP



PCH HAS INTERNAL WEAK PULL-DOWN

1 >TOP SWAP ENABLED
0 > TOP SWAP DISABLED (DEFAULT)

BOOT BIOS DEVICE



PCH INTERNAL PULL-DOWN.

1 > LPC / ESPI
0 > SPI (DEFAULT)

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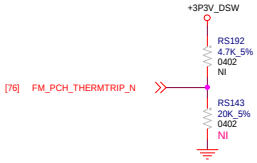
BOOT-HALT SEL STRAP

PCH HAS INTERNAL WEAK PULL-UP

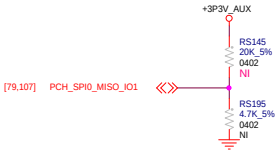
1 >BOOT HALT DISABLE
0 >BOOT HALT ENABLE

DCI ENABLE STRAP



PCH HAS INTERNAL WEAK PULL-DOWN

1 >DCI ENABLE
0 > DCI DISABLE



PCH HAS INTERNAL WEAK PULL-UP

1 >JTAG ODT ENABLE
0 >JTAG ODT DISABLE

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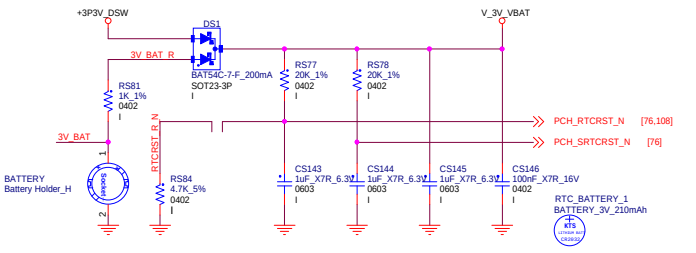
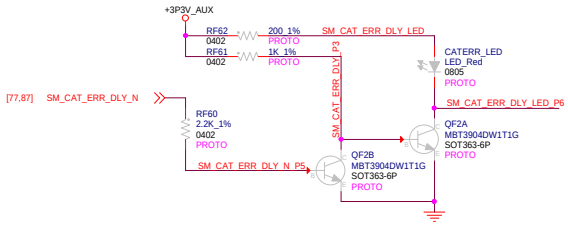
COMPUTRONICS IMAGE

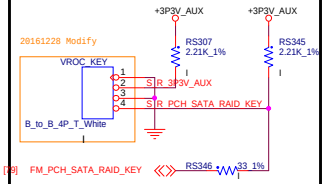
RTC BATTERY



CATERR LED

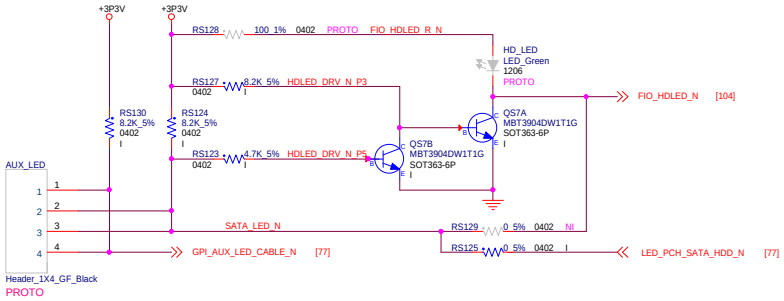


SATA RAID KEY



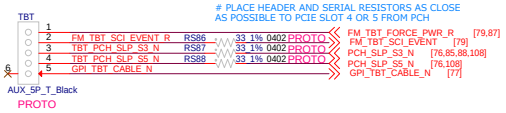
PCH KEY

AUX LED



[20150601] Delete RS122, AUX_PWR, RS121, QS6, DS2, RS120.
The CPLD will display INTR on the onboard display when INTRUDER is detected. No need for this external LED circuitry.

THUNDERBOLT SIDEBAND



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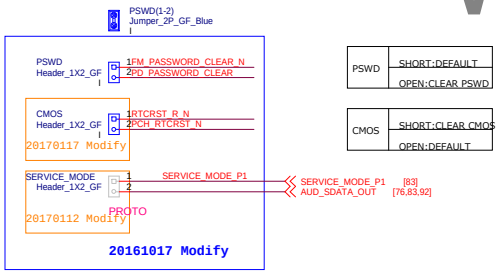
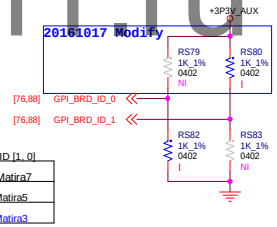
PW_CMOS_SERVICE Jumper



PSWD	SHORT:DEFAULT
	OPEN:CLEAR PSWD

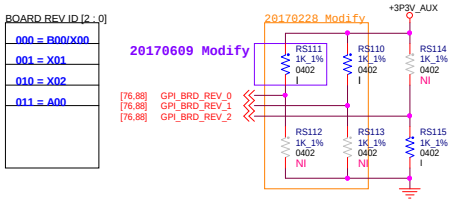
CMOS	SHORT:CLEAR CMOS
	OPEN:DEFAULT

BOARD ID

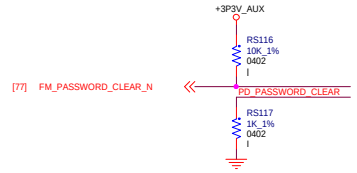


BOARD ID [1, 0]
00 = Matira7
01 = Matira5
10 = Matira3

BOARD REVISION ID



PASSWORD JUMPER



AMT DEBUG HOOK

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TITLE	Miscellaneous		
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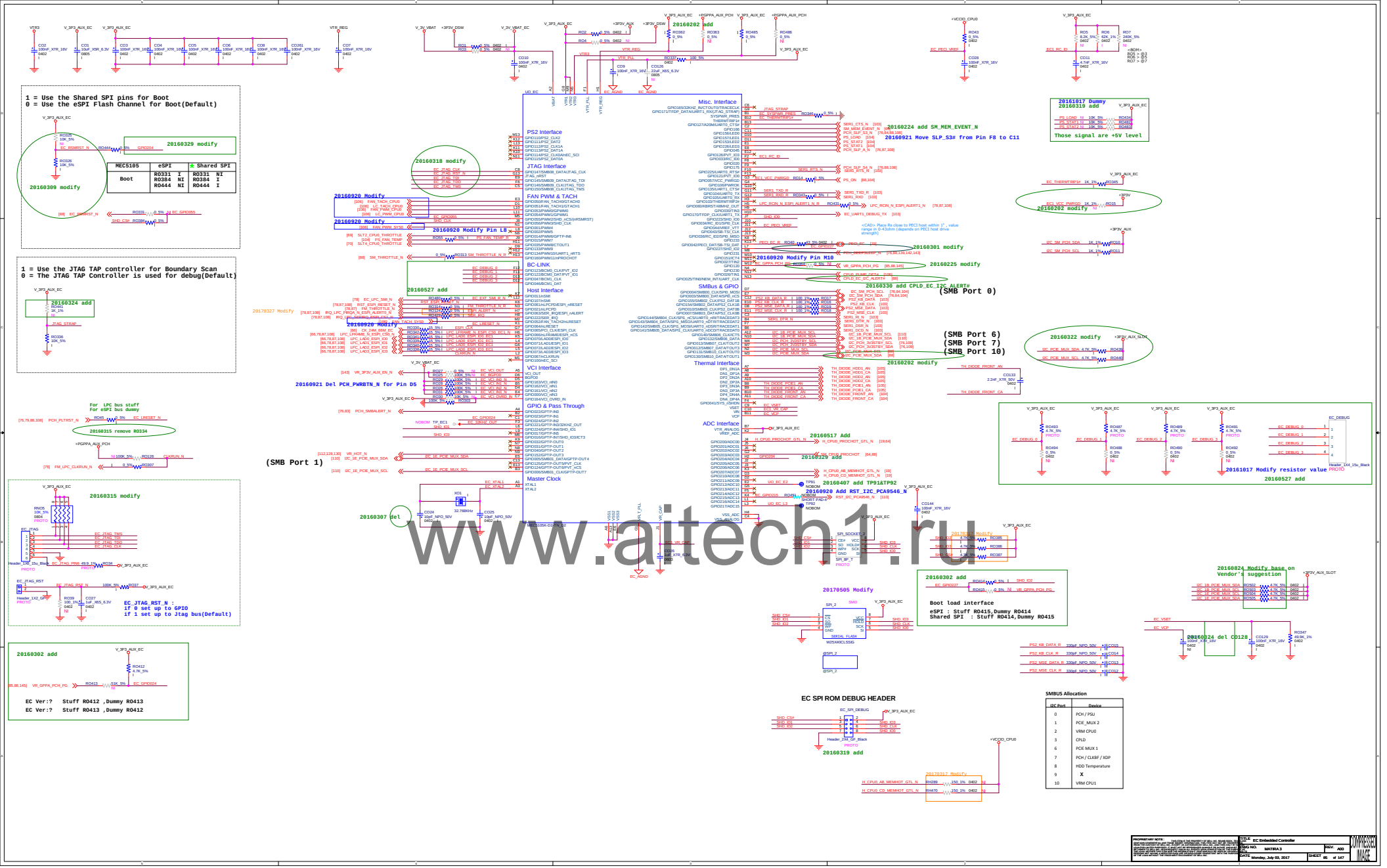
COMPUTER IMAGE



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TITLE	BLANK		
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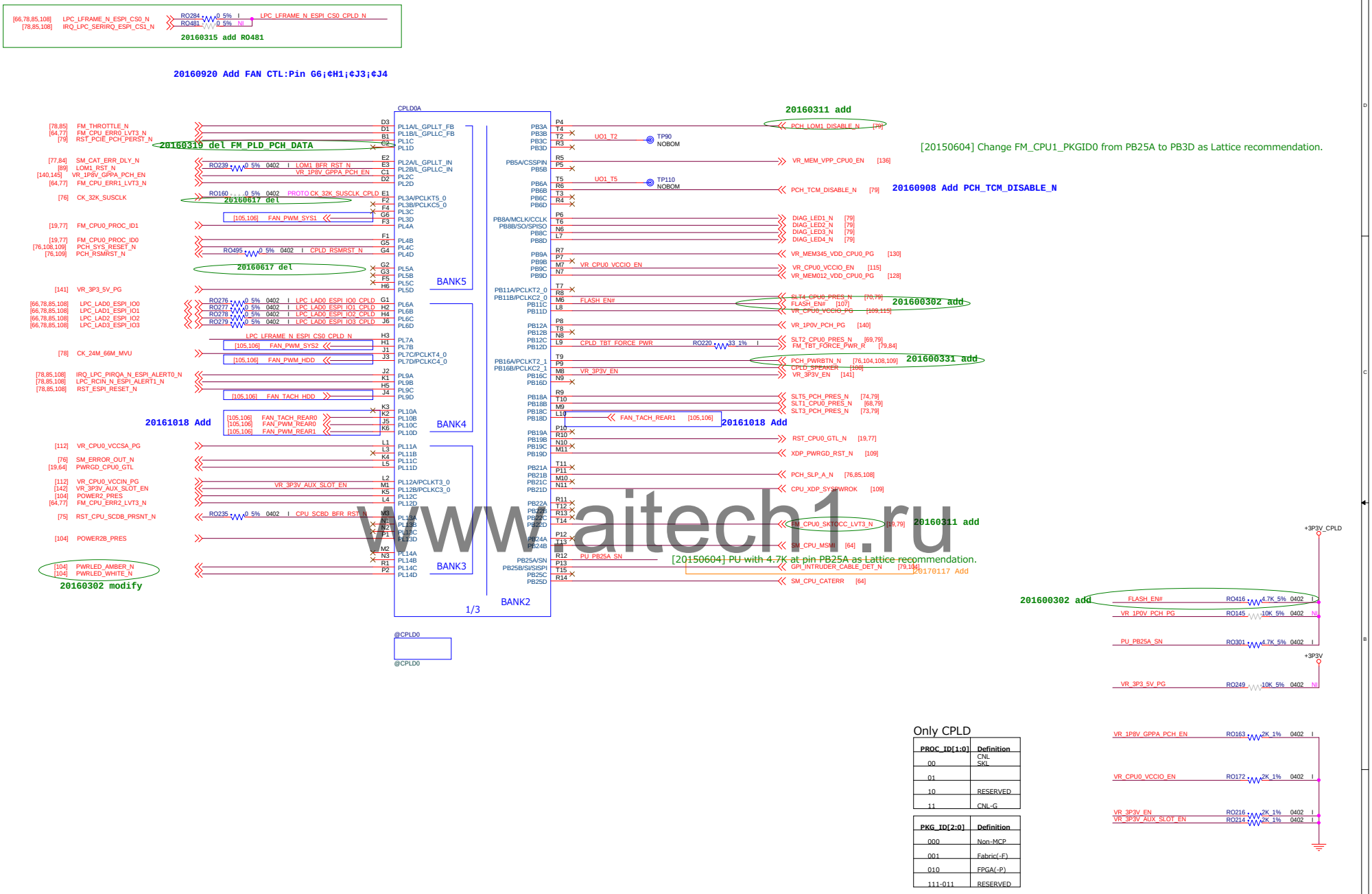
COMPRESSED IMAGE



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Only CPLD

PROC_ID[1:0]	Definition
00	CNL SKL
01	
10	RESERVED
11	CNL-G

PKG_ID[2:0]	Definition
000	Non-MCP
001	Fabric(-F)
010	FPGA(-P)
111-011	RESERVED

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20160920 Add FAN CTL:Pin G11¡¢H12

CPLD0B

[76,109] PCH_SYS_PWROK — D14 PR1A
[76,79,85,108] PCH_PLTRST_N — E15 PR1B
C15 PR1C
[85] CPLD_EC_I2C_ALERT# — B16 PR1D
D16 PR2A
[76] FM_ADR_TRIGGER_N — E14 PR2B
[76] PCH_PWROK_PG — PCH_PWROK_PG — C16 PR2C
20160617 del — D15 PR2D
20160311 add
CPLD_INTRUDER_N — E16 PR3A
F15 PR3B
[64] CPLD_PROC_PWRGD — F13 PR3C
[143] V_5VAUX_MEM_CPU0_EN_N — G12 PR3D
[77] GPP_PCH_CPLD_G11 — RO308 0_5% 0402 I GPP_PCH_CPLD_G11_R — F14 PR4A
F16 PR4B
[77] GPP_PCH_CPLD_G10 — RO309 0_5% 0402 I GPP_PCH_CPLD_G10_R — F12 PR4C
G13 PR4D
G15 PR5A
G14 PR5B
[105,106] FAN_TACH_SYS1 — G11 PR5C
[105,106] FAN_TACH_SYS2 — H12 PR5D
MVU_RST_N — G16 PR6A
MVU_D1 — H15 PR6B
MVU_BL_N — H13 PR6C
MVU_D2 — J12 PR6D
MVU_A0 — H14 PR7A/PCLKT1_0
MVU_A1 — H16 PR7B/PCLKC1_0
MVU_D4 — J16 PR7C
MVU_D6 — J14 PR7D
MVU_D5 — J15 PR9A
MVU_WR_N — K16 PR9B
MVU_D0 — H11 PR9C
MVU_D3 — J13 PR9D
[76,84] GPI_BRD_ID_0 — K14 PR10A
[76,84] GPI_BRD_ID_1 — K15 PR10B
20160309 add
[85] EC_RSMRST_N — J11 PR10C
[143] VR_3P3V_AUX_PG — L12 PR10D
L16 PR11A
[79,82] GPI_PCH_HS_DET_N — L14 PR11B
[19] PWRGD_CPU0_AB_DRAM_GTL — K13 PR11C
[19] PWRGD_CPU0_CD_DRAM_GTL — K12 PR11D
L15 PR12A
[64] CPU0_FIVR_FAULT_LVT — M16 PR12B
K11 PR12C
FM_PLD_DBGBTN — L13 PR12D
M14 PR13A
[64] FM_CPU_THERMTRIP_LVT3_N — M15 PR13B
N15 PR13C
P16 PR13D
N16 PR14A
[85] SM_THROTTLE_N — N14 PR14B
[128,130] VR_MEM_VDD_CPU0_EN — VR_MEM_VDD_PVPP_CPU0_EN — P15 PR14C
[129,143] STBY_FROM_AUX_EN — STBY_FROM_AUX_EN — R16 PR14D

[20150729] To add two GPIOs (4A/4C) from PCH to CPLD for communication as Dell's request

PT9A C4
PT9B B5 TPM_BFR_RST_N — RO241 0_5% 0402 I — PCH_TPM_DISABLE_N [79]
PT9C B3 — TPM_RST_N [107] — PS_PG_3P3_N [104]
20160311 add
PT10A A4
PT10B C5 — PCH_SPKR [83,84]
20160920 Add PCH_SPKR
PT11A A5 PCIE1_S1_BFR_RST_N — RO227 0_5% 0402 I — PCIE1_SLOT1_RST_N [68]
PT11B B6 PCIE1_S2_BFR_RST_N — RO228 0_5% 0402 I — PCIE1_SLOT2_RST_N [69]
PT11C A3
PT11D B4 VR_MEM_VTT_DRVR_CPU0_EN — VR_MEM_VTT_DRVR_CPU0_EN [138]
PT12A D6 PCIE3_S3_BFR_RST_N — RO229 0_5% 0402 I — PCIE3_SLOT3_RST_N [73]
PT12B E7 — TCM_RST_N [66]
PT12C/TDO C6 CPLD_ISP_TDO
20160908 Add TCM_RST_N
PT12D/TDI A6 CPLD_ISP_TDI_R — RO200 33_1% 0402 I — CPLD_ISP_TDI
PT13A B7 PCIE1_S4_BFR_RST_N — RO230 0_5% 0402 I — PCIE1_SLOT4_RST_N [70]
PT13B C7 — GPI_BRD_REV_0 [76,84]
PT13C E6 — GPI_BRD_REV_1 [76,84]
PT13D D7 — GPI_BRD_REV_2 [76,84]
F7 PU_PLD_DEBUG_MODE_N
PT16A E8 ICT_TEST_CPLD — TP_ICT_CPLD1 NOBOM
PT16B A7 CPLD_ISP_TCK_R — RO202 33_1% 0402 I — CPLD_ISP_TCK
PT16C/TCK B8 CPLD_ISP_TMS_R — RO204 33_1% 0402 I — CPLD_ISP_TMS
PT16D/TMS
C8
PT17A/PCLKT0_1 A8 PCIE3_S5_BFR_RST_N — RO231 0_5% 0402 I — FM_ADR_COMPLETE [76]
PT17B/PCLKC0_1 D8 — PCIE3_SLOT5_RST_N [74]
PT17C E9 PCH_DEEPSLEEP_N
20160617 del
PT17D — PCH_DEEPSLEEP_N [76,85,139,142,143]
F8 UO1_TP1 — UO1_TP1 NOBOM
PT18A D9 PCIE2_S6_BFR_RST_N — RO232 0_5% 0402 I — PCIE2_SLOT6_RST_N [72]
PT18B A9 I2C_1A_CPLD_SCL_R — RO243 0_5% 0402 I — I2C_PCIE_MUX_SCL [85]
PT18C/SCL/PCLKT0_0 C9 I2C_1A_CPLD_SDA_R — RO244 0_5% 0402 I — I2C_PCIE_MUX_SDA [85]
PT18D/SDA/PCLKC0_0
B9
PT19A A10 VR_CPU0_VCCIN_EN — VR_CPU0_VCCIN_EN [112]
PT19B F9 — PS_ON [85,104]
PT19C E11 — VR_1P8V_PCH_PG [140]
PT19D
PT20A D10 CPLD_SUSWARN_N — RO529 0_5% 0402 I — PCH_SUSWARN_N [76]
PT20B E10 — FM_ESPI_EN [83,145]
PT20C/JTAGENB C10 CPLD_SUSACK_N — RO530 0_5% 0402 I — PCH_SUSACK_N [76]
PT20D/PROGRAMN B10 PU_PT20D_PROGRAMN
20170316 Add
[20150604] PU with 4.7K at pin PT20D as Lattice recommendation.
A11
PT21A C11 — VR_MAIN_EN [141]
PT21B F10
20160617 del
PT21C D11 — PCH_SLP_S3_N [76,84,85,108]
PT21D — VR_GPPA_PCH_PG [85,145]
B11
PT22A A12
PT22B B13
Don't use it for M5 need
PT22C A14 VR_1P0V_PCH_EN — VR_1P0V_PCH_EN [140]
PT22D
C12
PT23A — PCH_SLP_S4_N [76,85,108]
PT23B B12 — CPLD_UART_DEBUG_TX [103]
B14
PT24A A15 — PCH_PHOT_N [76]
PT24B A13 SM_CPU0_PROCHOT_CPLD — RO218 0_5% 0402 I — AUX_FROM_MAIN_N [104]
PT24C/INITN — SM_CPU0_PROCHOT [64,85]
PT24D/DONE C13

[20150604] Change PCH_PHOT_N from PT20D to PT24A as Lattice recommendation.

BANK1 BANK0 2/3

+3P3V_CPLD
RO242 10K_5% 0402 I
CPLD_INTRUDER_N — CRO1 BAT54HT1G_200mA — PCH_INTRUDER_N [79,104]

FM_ADR_TRIGGER_N — RH221 10K_1% 0402 NI
PCH_PWROK_PG — RO178 2K_1% 0402 I
VR_MEM_VTT_DRVR_CPU0_EN — RO189 2K_1% 0402 I
VR_MEM_VDD_CPU0_EN — RO191 2K_1% 0402 I
VR_CPU0_VCCIN_EN — RO194 2K_1% 0402 I
VR_1P0V_PCH_EN — RO212 2K_1% 0402 I
STBY_FROM_AUX_EN — RO215 2K_1% 0402 I

+3P3V_CPLD
PU_PT20D_PROGRAMN — RO302 4.7K_5% 0402 I

+3P3V_CPLD
RO445 10K_5% — CPLD_EC_I2C_ALERT#

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CPLD DEBUG BUTTON

+3P3V_CPLD
RO184 10K_5% 0402 I
SW_RESET2 PROTO
DB1 TS-1187A-B-A-B-B-00-R-D-G
FM_PLD_DBGBTN
CO82 100nF_X7R_16V 0402 NI
<DESIGN > UNSTUFFED CAP DUE TO INTERNAL CPLD DEBOUNCING

MVU DISPLAY

Modify 11/3

+5V_AUX +5V
FBO5 600_500mA PROTO
FBO6 600_500mA NI

F_DISP
MVU_D0 5 D0 — VCC 4 — V_5V_MVU_DISP
MVU_D1 6 D1 — WR_N 1 — MVU_WR_N
MVU_D2 7 D2 — A1 2 — MVU_A1
MVU_D3 8 D3 — A0 3 — MVU_A0
MVU_D4 9 D4 — BL_N 12 — MVU_BL_N
MVU_D5 10 D5 — CLR_N 13 — MVU_RST_N
MVU_D6 11 D6 — GND 14
SLG2016 PROTO

CO81 100nF_X7R_16V 0402 PROTO

PLD PROGRAMMING HEADER

+3P3V_CPLD
20170118 Modify
DO3 1N5819HW-7-F_1A SOD123-2P

CPLD_JTAG1
P3V3_AUX_PLD_D 1
CPLD_ISP_TDO 2
CPLD_ISP_TDI 3
4
5
CPLD_ISP_TMS 6
7
CPLD_ISP_TCK 8
Header_1X8_GF PROTO

+3P3V_CPLD
20170118 Modify
RO195 10K_5% 0402 — CPLD_ISP_TDO
RO201 10K_5% 0402 — CPLD_ISP_TDI
RO205 10K_5% 0402 — CPLD_ISP_TMS
RO203 10K_5% 0402 — CPLD_ISP_TCK

RO198 475_1% 0402 I — GPI_CPLD_TDO [78]
RO199 475_1% 0402 I — GPO_CPLD_TDI [78]
RO197 475_1% 0402 I — GPO_CPLD_TMS [78]
RO196 475_1% 0402 I — GPO_CPLD_TCK [78]

+3P3V_CPLD
RO206 10K_5% 0402 I
PU_PLD_DEBUG_MODE_N
RO207 1K_1% 0402 NI

+3P3V_CPLD
CO85 10uF_X6S_6.3V 0603 I
CO84 100nF_X7R_16V 0402 I
20170118 Modify

+3P3V_CPLD +3P3V_AUX +3P3V_DSW
RNO9 0_5% 1206 I
RNO10 0_5% 1206 NI

CPLD0C
K10 VCC<7>
K7 VCC<6>
G10 VCC<5>
G7 VCC<4>
T16 VCC<3>
T1 VCC<2>
A16 VCC<1>
A1 VCC<0>
+PGPPA_AUX_PCH
E4 VCCIO5<0>
H7 VCCIO4<1>
J7 VCCIO4<0>
M4 VCCIO3<0>
N5 VCCIO2<3>
K8 VCCIO2<2>
N12 VCCIO2<1>
K9 VCCIO2<0>
M13 VCCIO1<3>
J10 VCCIO1<2>
H10 VCCIO1<1>
E13 VCCIO1<0>
D5 VCCIO0<3>
G9 VCCIO0<2>
D12 VCCIO0<1>
G8 VCCIO0<0>
NC<0> A2
R15 GND<23>
R2 GND<22>
P14 GND<21>
P3 GND<20>
N13 GND<19>
N4 GND<18>
M12 GND<17>
M5 GND<16>
L11 GND<15>
L6 GND<14>
J9 GND<13>
J8 GND<12>
H9 GND<11>
H8 GND<10>
F11 GND<9>
F6 GND<8>
E12 GND<7>
E5 GND<6>
D13 GND<5>
D4 GND<4>
C14 GND<3>
C3 GND<2>
B15 GND<1>
B2 GND<0>
3/3

+3P3V_CPLD
CO086 100nF_X7R_16V 0402 I
CO087 100nF_X7R_16V 0402 I
CO088 100nF_X7R_16V 0402 I
CO089 100nF_X7R_16V 0402 I
CO090 100nF_X7R_16V 0402 I
CO091 100nF_X7R_16V 0402 I
CO092 100nF_X7R_16V 0402 I

+3P3V_CPLD
CO093 100nF_X7R_16V 0402 I
CO094 100nF_X7R_16V 0402 I
CO095 100nF_X7R_16V 0402 I
CO097 100nF_X7R_16V 0402 I
CO096 100nF_X7R_16V 0402 I
CO098 100nF_X7R_16V 0402 I
CO099 100nF_X7R_16V 0402 I

+3P3V_CPLD
CO100 100nF_X7R_16V 0402 I
CO101 100nF_X7R_16V 0402 I
CO102 100nF_X7R_16V 0402 I
CO103 100nF_X7R_16V 0402 I
CO106 10nF_X7R_16V 0402 I

+PGPPA_AUX_PCH
CO104 100nF_X7R_16V 0402 I
CO105 100nF_X7R_16V 0402 I

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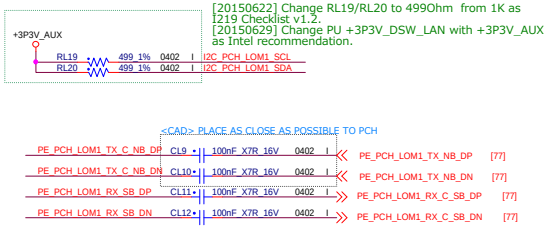
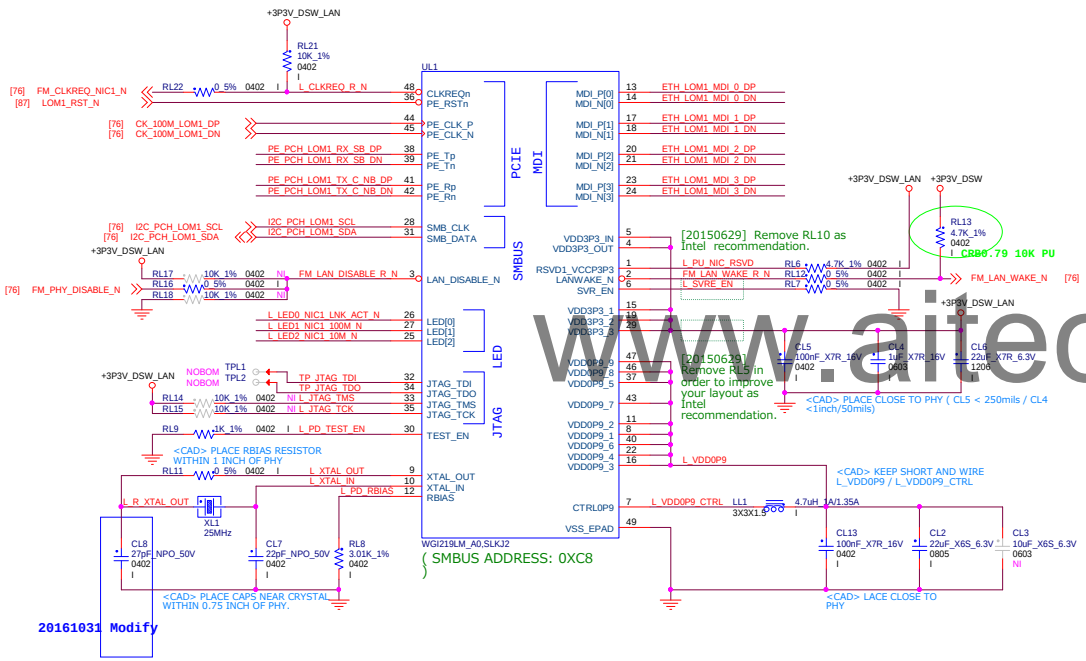
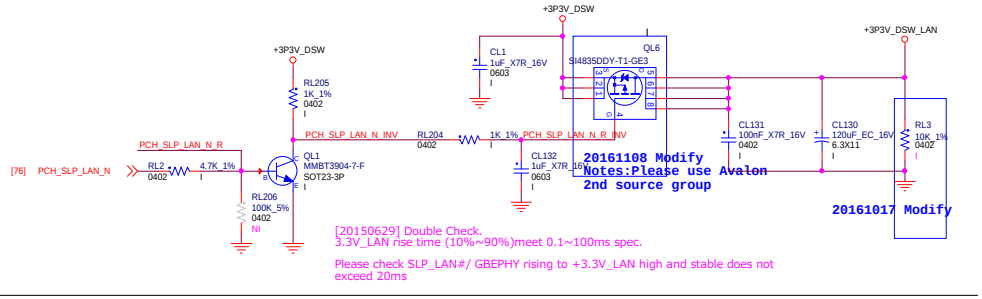
COMPRESSED IMAGE

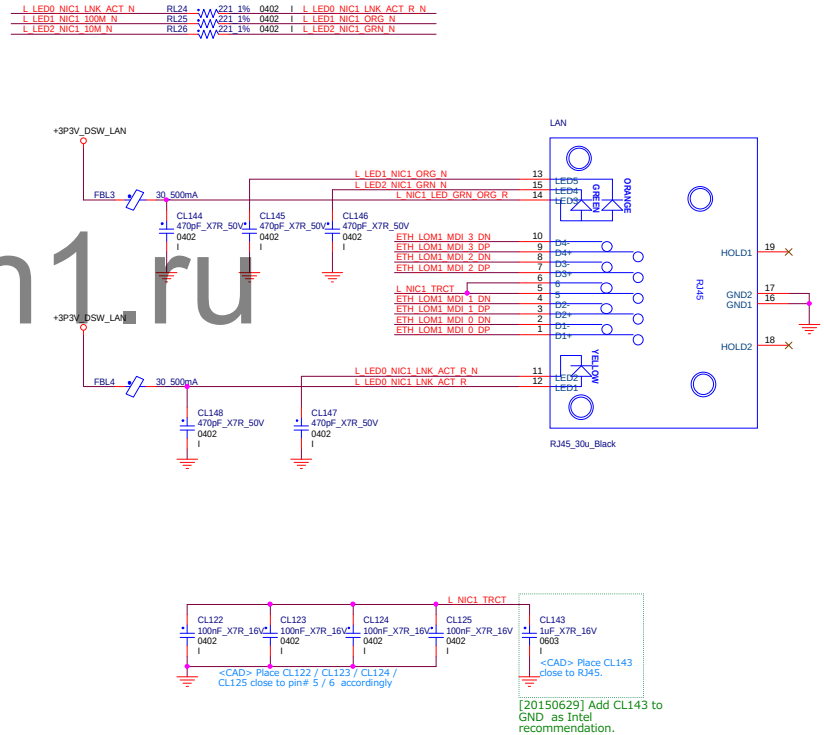
Jacksonville / I219 (PHY)





I219 LOM Power





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TITLE	GBE I219 Jacksonville		
DWG NO.	MATIRA 3	REV.	A00
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TITLE	BLANK		
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COMPRESSED IMAGE

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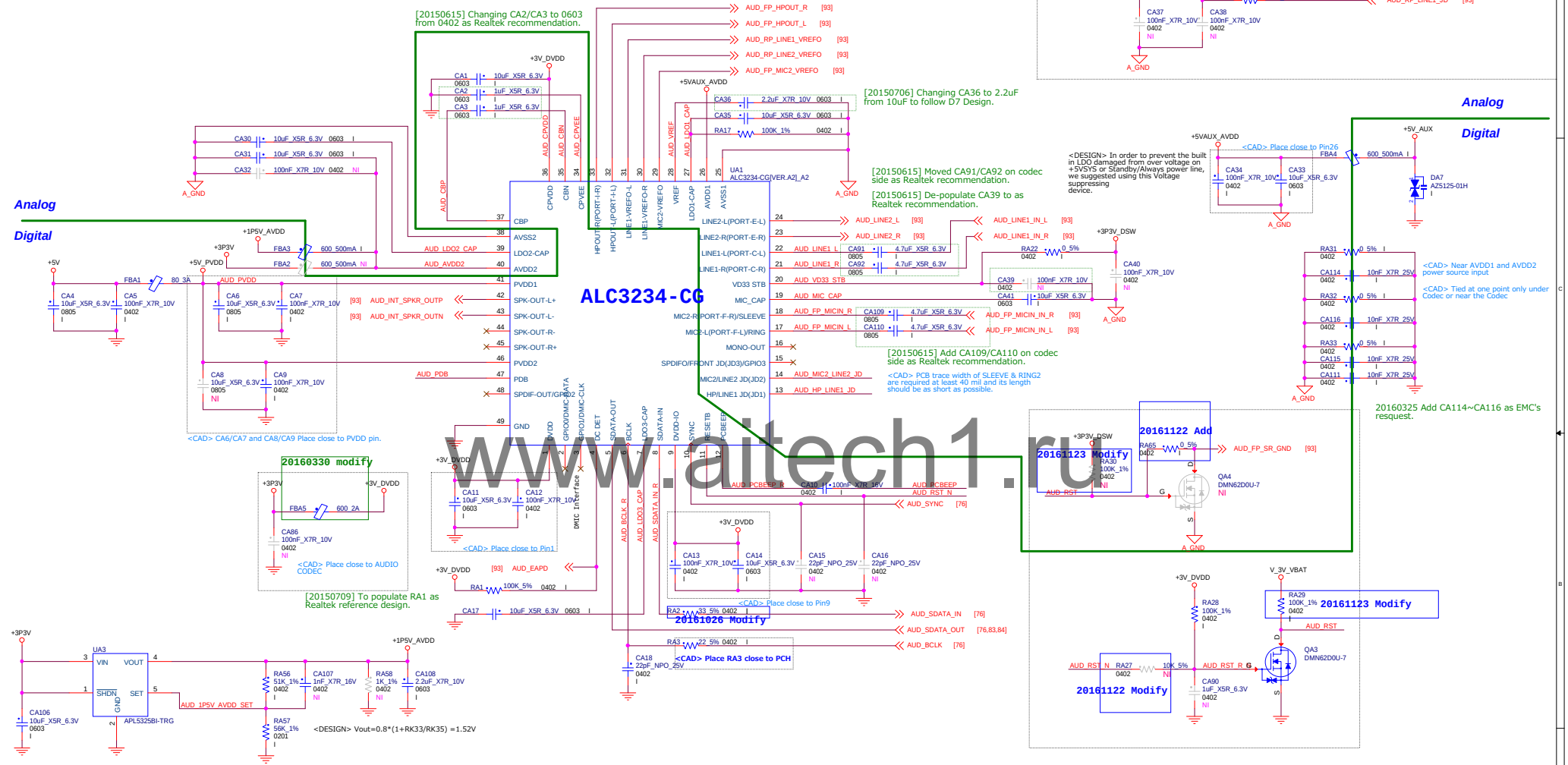
COMPRESSED IMAGE

Audio Codec



Amplifier Power Down Options

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TITLE	Audio Codec		
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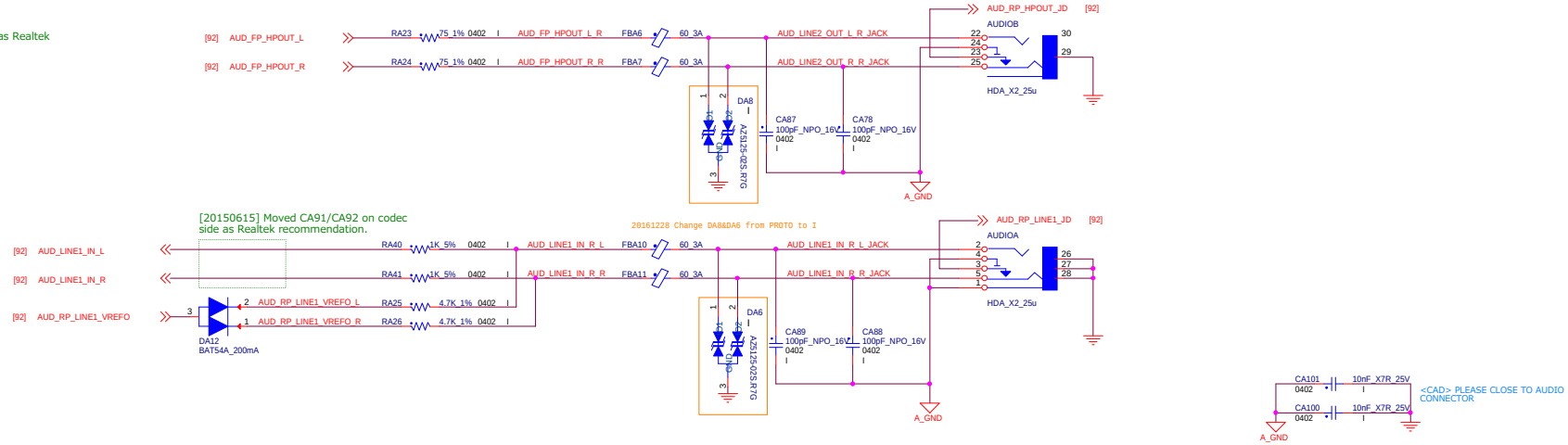
REAR PANEL

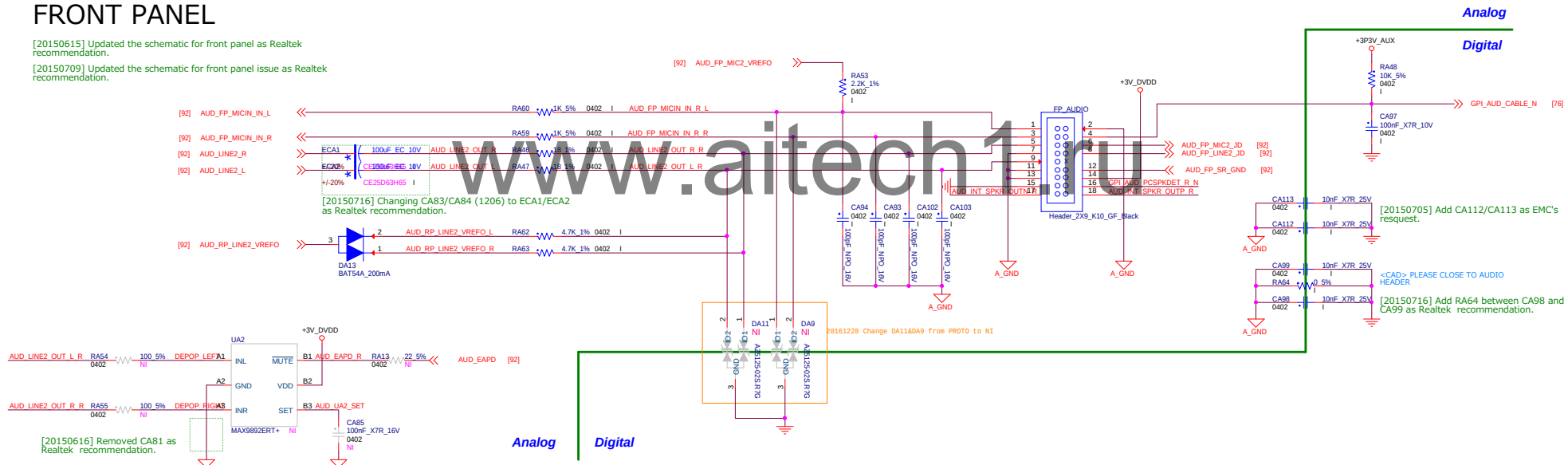
[20150709] Updated the schematic for Rear Panel as Realtek recommendation.



FRONT PANEL

[20150615] Updated the schematic for front panel as Realtek recommendation.

[20150709] Updated the schematic for front panel issue as Realtek recommendation.



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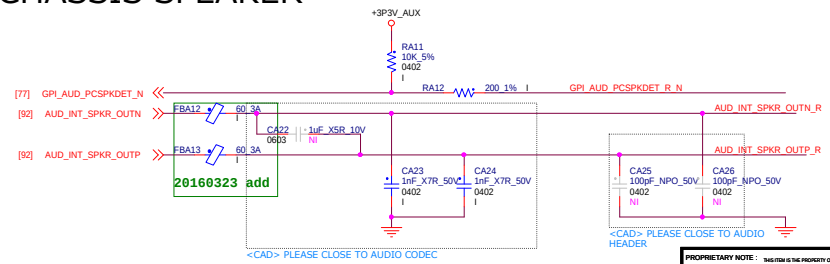
ARD v0.25

COMPRESSED IMAGE

CHASSIS SPEAKER



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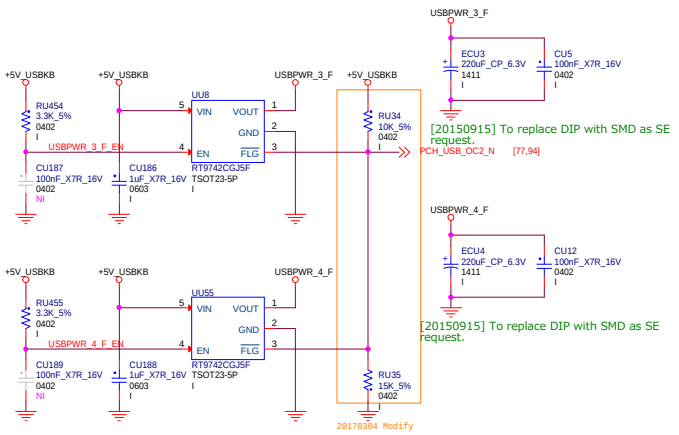
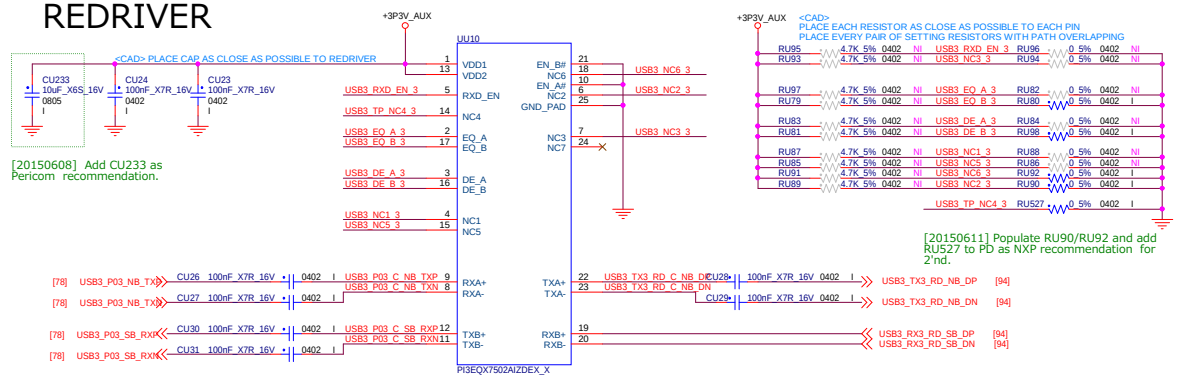
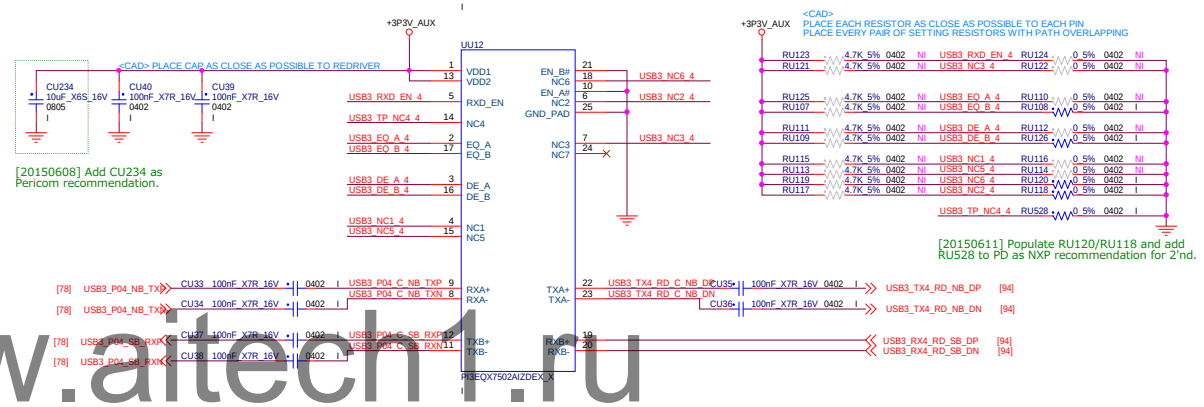
COMPRESSED IMAGE

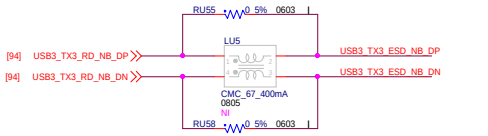
Rear USB3.0 Connector 1OF3

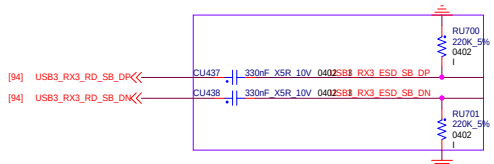


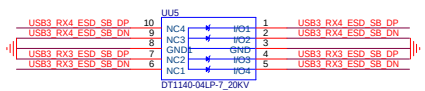
USB3.0 REDRIVER

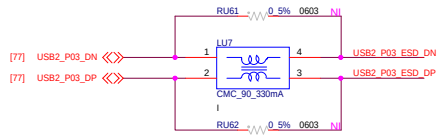


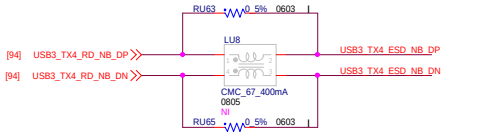


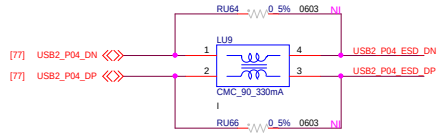


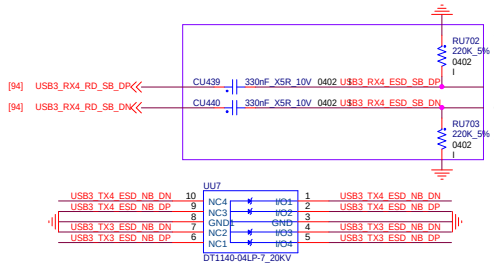


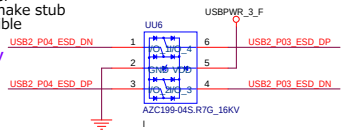


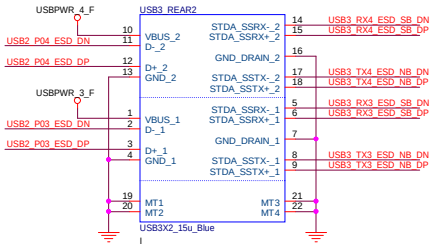












Pin Strap Table - Pericom

EQ_x	@2.5GHz
Pin#2	CHA
Pin#17	CHB
0	3dB
NC	6dB
1	9dB

DE_x	
Pin#3	CHA
Pin#16	CHB
0	0dB
NC	-3.5dB
1	-6dB

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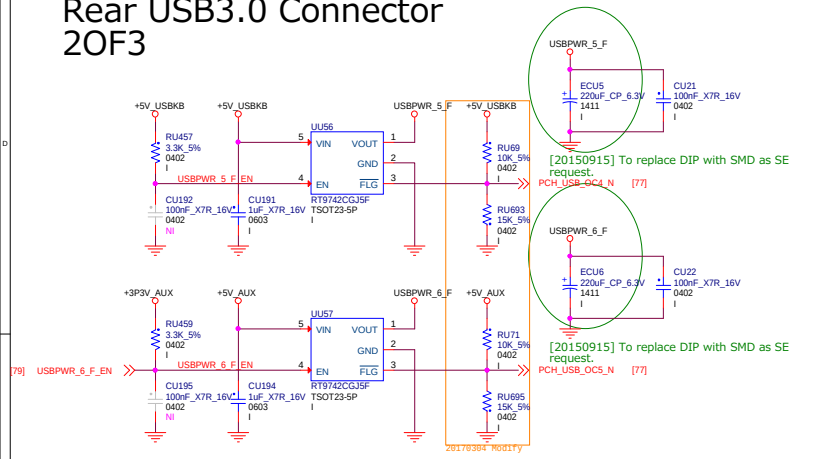
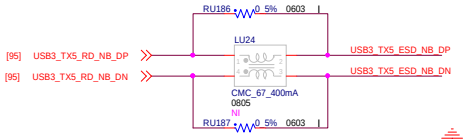
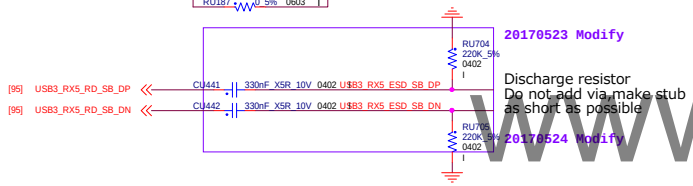
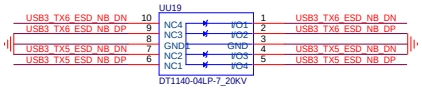
UNCLASSIFIED IMAGE

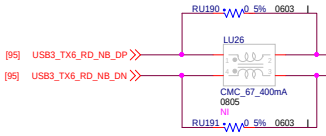
Rear USB3.0 Connector 2OF3

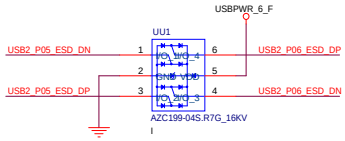


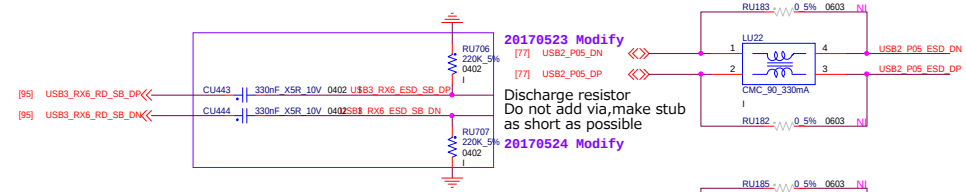


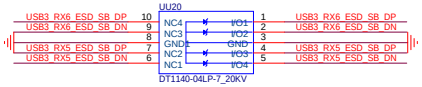


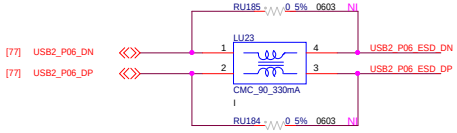




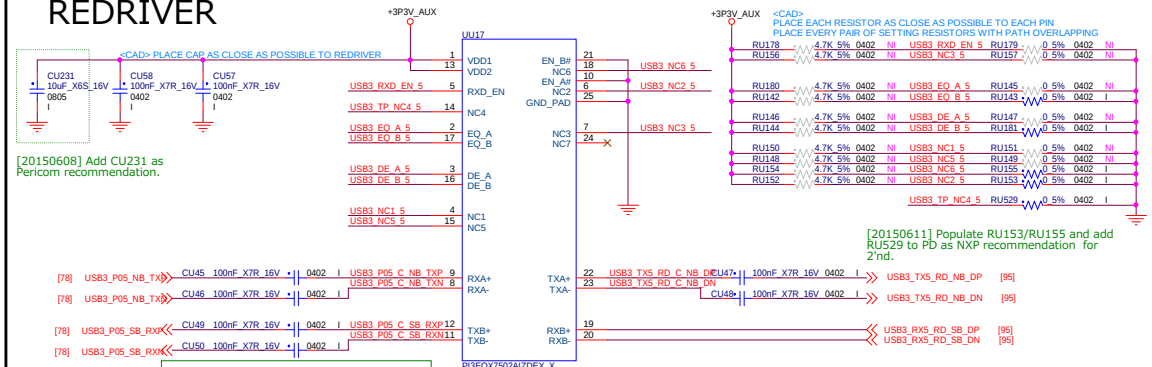


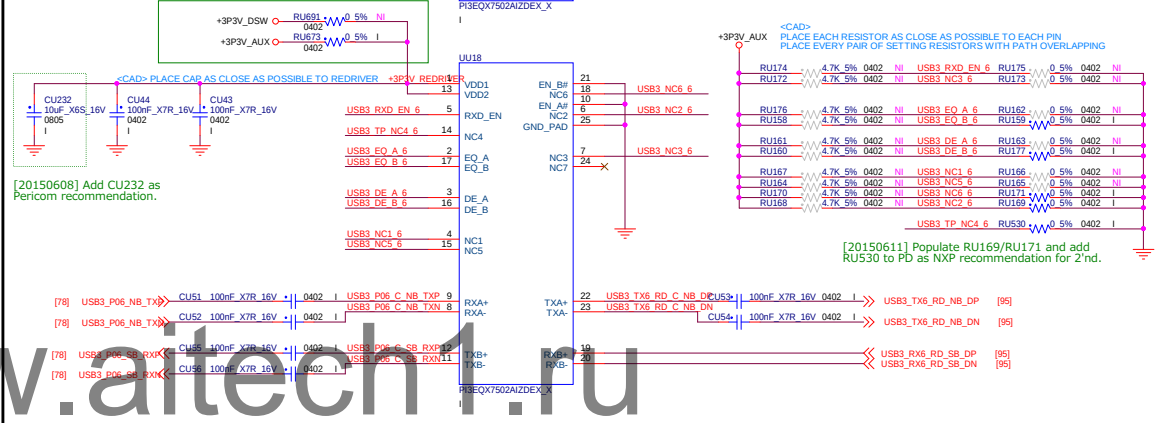


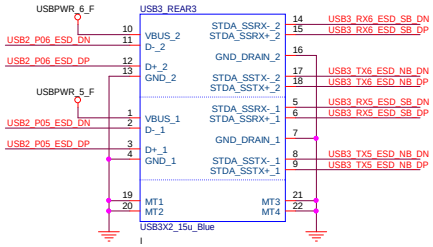




USB3.0 REDRIVER







Pin Strap Table - Pericom

EQ_x	@2.5GHz
Pin#2	CHA
Pin#17	CHB
0	3dB
NC	6dB
1	9dB

DE_x	
Pin#3	CHA
Pin#16	CHB
0	0dB
NC	-3.5dB
1	-6dB

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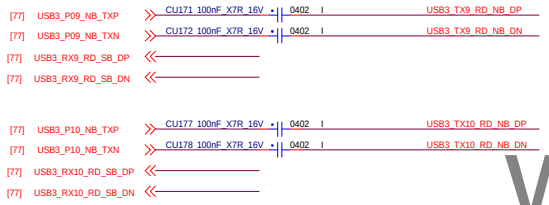
COMPUTER SYSTEMS IMAGE

Front Panel USB3.0 Connector(Blue) For FIO SD Card&USB Hub

20160428
Power Switch and ESD component change to FIO



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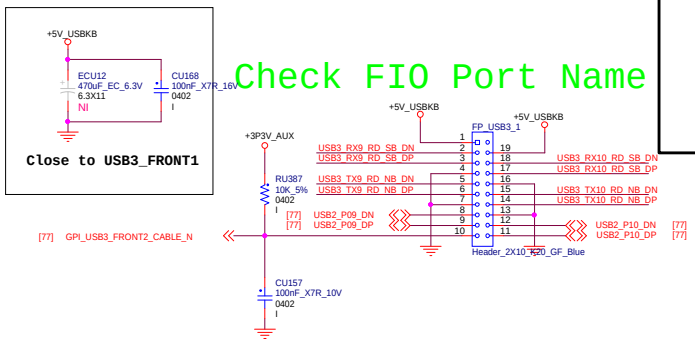

Pin Strap Table - Pericom

EQ_x	@2.5GHz
Pin#2	CHA
Pin#17	CHB
0	3dB
NC	6dB
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DE_x	
Pin#3	CHA
Pin#16	CHB
0	0dB
NC	-3.5dB
1	-6dB

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TITLE	Front Panel USB3_1		
DWG NO.	MATIRA 3	REV.	A00
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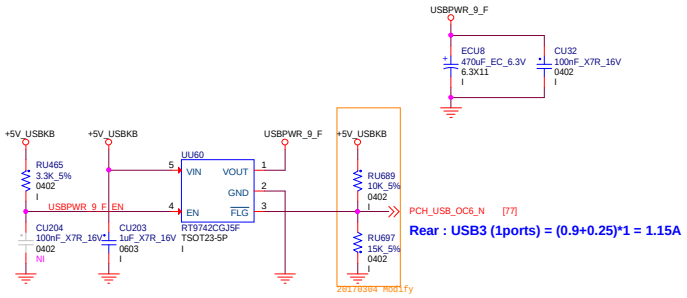
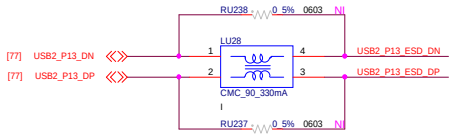
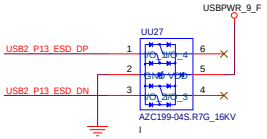
COMPRESSED IMAGE

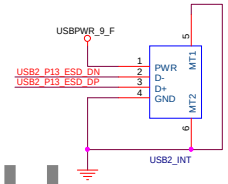
INT USB2.0 Connector



Rear : USB3 (1ports) = (0.9+0.25)*1 = 1.15A







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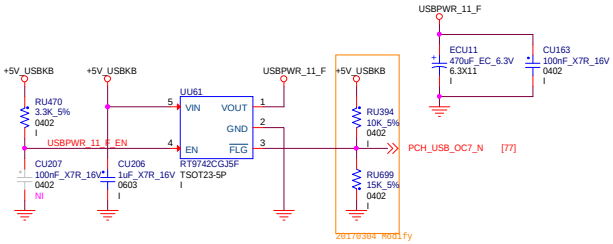
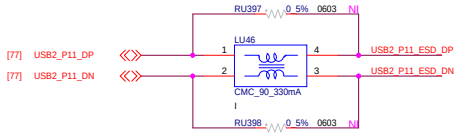
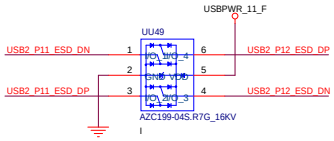
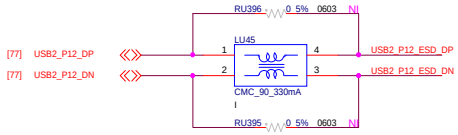
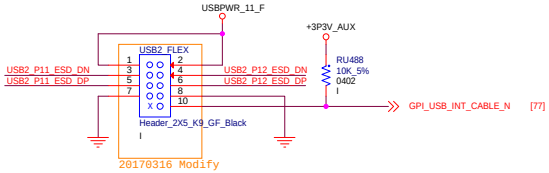
INT USB2.0 Card Reader Header











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TITLE	INT USB 2.0
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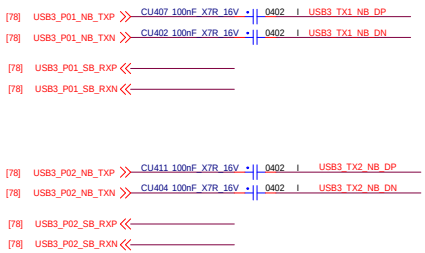
COMPRESSED IMAGE

Front Panel USB3.0
Connector(Black)
For FIO TypeC

20160428
Power Switch and ESD component change to FIO

20161117
Remove Redriver to FIO



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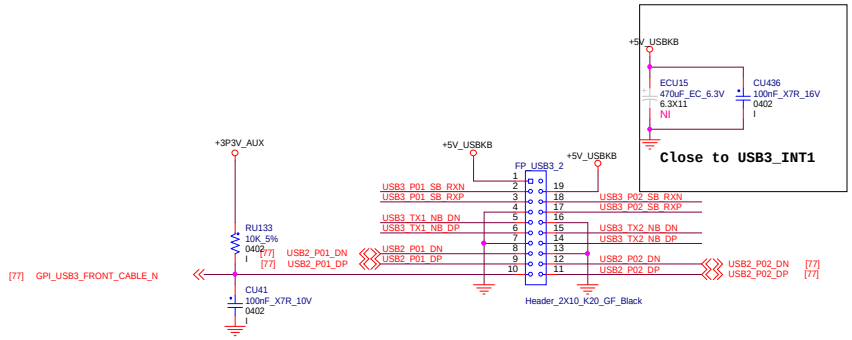

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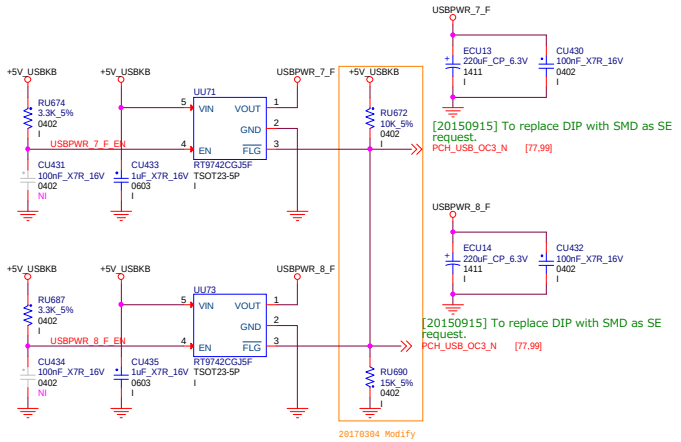
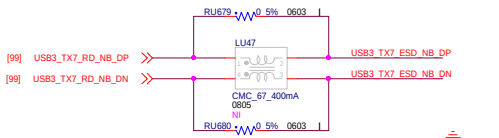
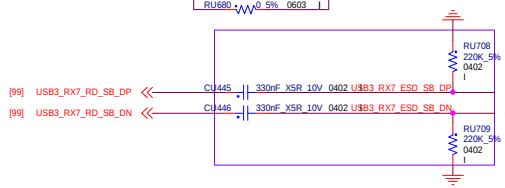
TITLE	Front Panel USB3_2		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	98 of 147

COMPRESSED IMAGE

Rear USB3.0 Connector 1OF2



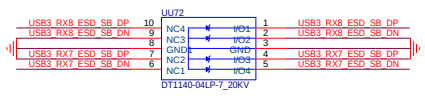


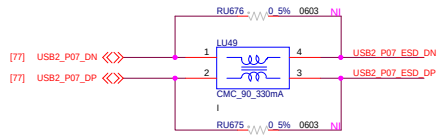


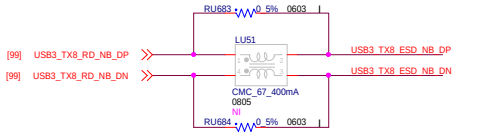
20170523 Modify

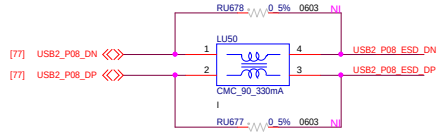
Discharge resistor
Do not add via,make stub
as short as possible

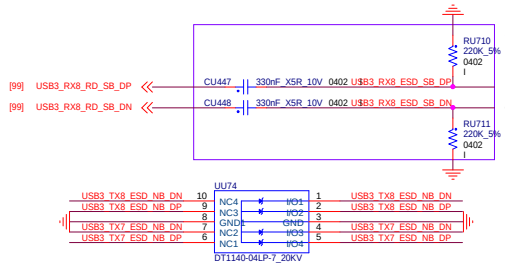
20170524 Modify







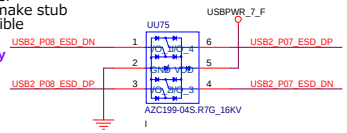


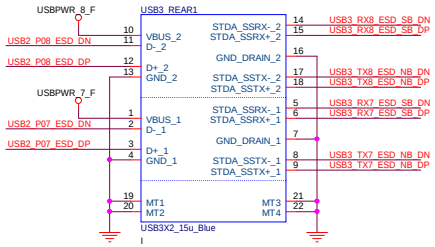


20170523 Modify

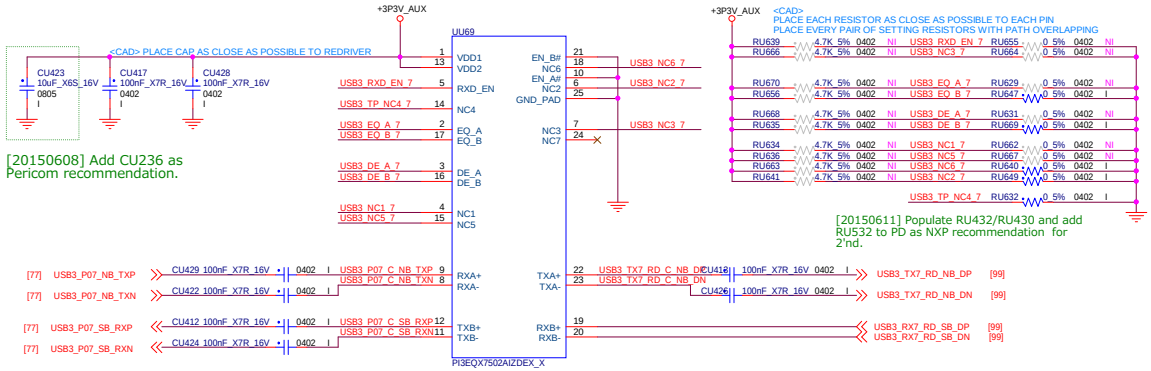
Discharge resistor
Do not add via,make stub
as short as possible

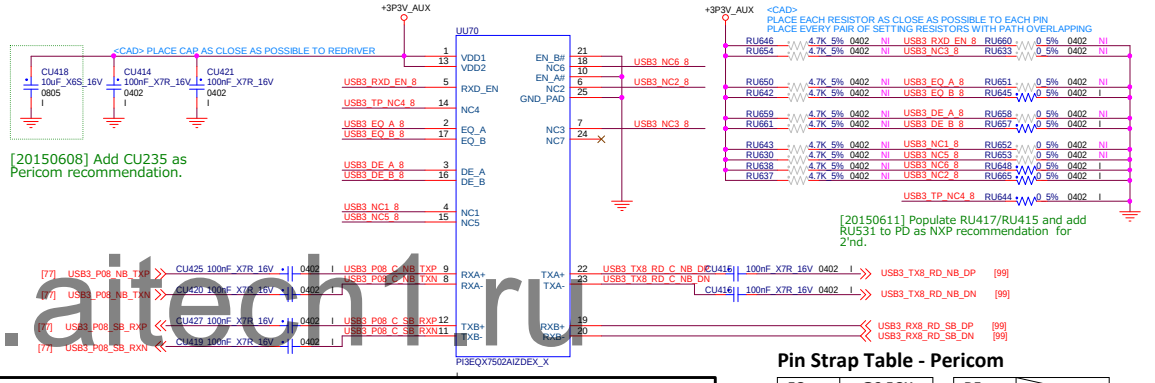
20170524 Modify





USB3.0 REDRIVER





Pin Strap Table - Pericom

EQ_x	@2.5GHz
Pin#2	CHA
Pin#17	CHB
0	3dB
NC	6dB
1	9dB

DE_x	
Pin#3	CHA
Pin#16	CHB
0	0dB
NC	-3.5dB
1	-6dB

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TITLE	USB 3.0 Connector - 3 OF 3		
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TITLE	Blank		
DWG NO.	MATIRA 3	REV.	A00
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COMPRESSED IMAGE

SATA Connector

20170112 Modify

[77] SATA6G_PCH_P0_RX_SB_DP	RT15	10nF_X7R_16V	0402	I	SATA6G_PCH_P0_RX_C_SB_DP	SATA6G_PCH_P0_RX_C_SB_DP	SATA0
[77] SATA6G_PCH_P0_RX_SB_DN	RT16	10nF_X7R_16V	0402	I	SATA6G_PCH_P0_RX_C_SB_DN	SATA6G_PCH_P0_RX_C_SB_DN	
[77] SATA6G_PCH_P0_TX_NB_DN	CT2	10nF_X7R_16V	0402	I	SATA6G_PCH_P0_TX_C_NB_DN	SATA6G_PCH_P0_TX_C_NB_DN	
[77] SATA6G_PCH_P0_TX_NB_DP	CT1	10nF_X7R_16V	0402	I	SATA6G_PCH_P0_TX_C_NB_DP	SATA6G_PCH_P0_TX_C_NB_DP	
[77] SATA6G_PCH_P1_RX_SB_DP	RT41	10nF_X7R_16V	0402	I	SATA6G_PCH_P1_RX_C_SB_DP	SATA6G_PCH_P1_RX_C_SB_DP	SATA1
[77] SATA6G_PCH_P1_RX_SB_DN	RT42	10nF_X7R_16V	0402	I	SATA6G_PCH_P1_RX_C_SB_DN	SATA6G_PCH_P1_RX_C_SB_DN	
[77] SATA6G_PCH_P1_TX_NB_DN	CT32	10nF_X7R_16V	0402	I	SATA6G_PCH_P1_TX_C_NB_DN	SATA6G_PCH_P1_TX_C_NB_DN	
[77] SATA6G_PCH_P1_TX_NB_DP	CT31	10nF_X7R_16V	0402	I	SATA6G_PCH_P1_TX_C_NB_DP	SATA6G_PCH_P1_TX_C_NB_DP	
[77] SATA6G_PCH_P2_RX_SB_DP	RT17	10nF_X7R_16V	0402	I	SATA6G_PCH_P2_RX_C_SB_DP	SATA6G_PCH_P2_RX_C_SB_DP	SATA2
[77] SATA6G_PCH_P2_RX_SB_DN	RT18	10nF_X7R_16V	0402	I	SATA6G_PCH_P2_RX_C_SB_DN	SATA6G_PCH_P2_RX_C_SB_DN	
[77] SATA6G_PCH_P2_TX_NB_DN	CT6	10nF_X7R_16V	0402	I	SATA6G_PCH_P2_TX_C_NB_DN	SATA6G_PCH_P2_TX_C_NB_DN	
[77] SATA6G_PCH_P2_TX_NB_DP	CT5	10nF_X7R_16V	0402	I	SATA6G_PCH_P2_TX_C_NB_DP	SATA6G_PCH_P2_TX_C_NB_DP	
[77] SATA6G_PCH_P3_RX_SB_DP	RT13	10nF_X7R_16V	0402	I	SATA6G_PCH_P3_RX_C_SB_DP	SATA6G_PCH_P3_RX_C_SB_DP	SATA3
[77] SATA6G_PCH_P3_RX_SB_DN	RT14	10nF_X7R_16V	0402	I	SATA6G_PCH_P3_RX_C_SB_DN	SATA6G_PCH_P3_RX_C_SB_DN	
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[77] SATA6G_PCH_P4_RX_SB_DP	RT23	10nF_X7R_16V	0402	I	SATA6G_PCH_P4_RX_C_SB_DP	SATA6G_PCH_P4_RX_C_SB_DP	SATA4
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[77] SATA6G_PCH_P5_TX_NB_DN	CT12	10nF_X7R_16V	0402	I	SATA6G_PCH_P5_TX_C_NB_DN	SATA6G_PCH_P5_TX_C_NB_DN	
[77] SATA6G_PCH_P5_TX_NB_DP	CT11	10nF_X7R_16V	0402	I	SATA6G_PCH_P5_TX_C_NB_DP	SATA6G_PCH_P5_TX_C_NB_DP	
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[77] SATA6G_PCH_P6_RX_SB_DN	RT22	10nF_X7R_16V	0402	I	SATA6G_PCH_P6_RX_C_SB_DN	SATA6G_PCH_P6_RX_C_SB_DN	
[77] SATA6G_PCH_P6_TX_NB_DN	CT14	10nF_X7R_16V	0402	I	SATA6G_PCH_P6_TX_C_NB_DN	SATA6G_PCH_P6_TX_C_NB_DN	
[77] SATA6G_PCH_P6_TX_NB_DP	CT13	10nF_X7R_16V	0402	I	SATA6G_PCH_P6_TX_C_NB_DP	SATA6G_PCH_P6_TX_C_NB_DP	
[77] SATA6G_PCH_P7_RX_SB_DP	RT25	10nF_X7R_16V	0402	I	SATA6G_PCH_P7_RX_C_SB_DP	SATA6G_PCH_P7_RX_C_SB_DP	ODD1
[77] SATA6G_PCH_P7_RX_SB_DN	RT26	10nF_X7R_16V	0402	I	SATA6G_PCH_P7_RX_C_SB_DN	SATA6G_PCH_P7_RX_C_SB_DN	
[77] SATA6G_PCH_P7_TX_NB_DN	CT16	10nF_X7R_16V	0402	I	SATA6G_PCH_P7_TX_C_NB_DN	SATA6G_PCH_P7_TX_C_NB_DN	
[77] SATA6G_PCH_P7_TX_NB_DP	CT15	10nF_X7R_16V	0402	I	SATA6G_PCH_P7_TX_C_NB_DP	SATA6G_PCH_P7_TX_C_NB_DP	

Pin	Signal
9	HOLD2
7	GND3
6	B+
5	B-
4	GND2
3	A-
2	A+
1	GND1
8	HOLD1

SATA_S_15u_Blue
SATA_S_15u_Black
SATA_S_15u_Black
SATA_S_15u_Black
SATA_S_15u_Black
SATA_S_15u_Black
SATA_S_15u_White
SATA_S_15u_Black

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TITLE	SATA Connector		
DWG NO.	MATIRA 3	REV.	A00
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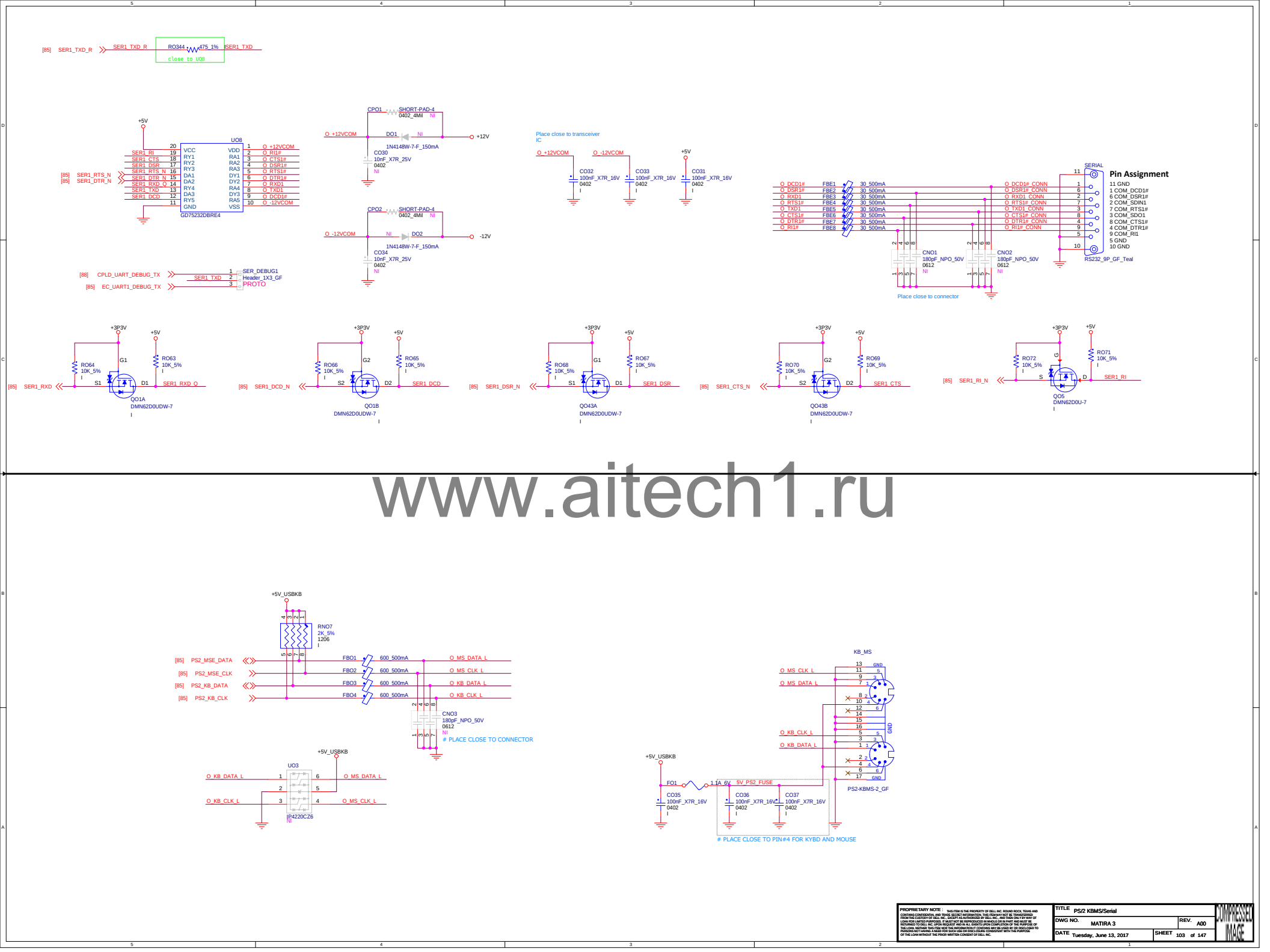
COMPUTER SECURITY IMAGE



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TITLE	PS/2 KBMS/Serial		
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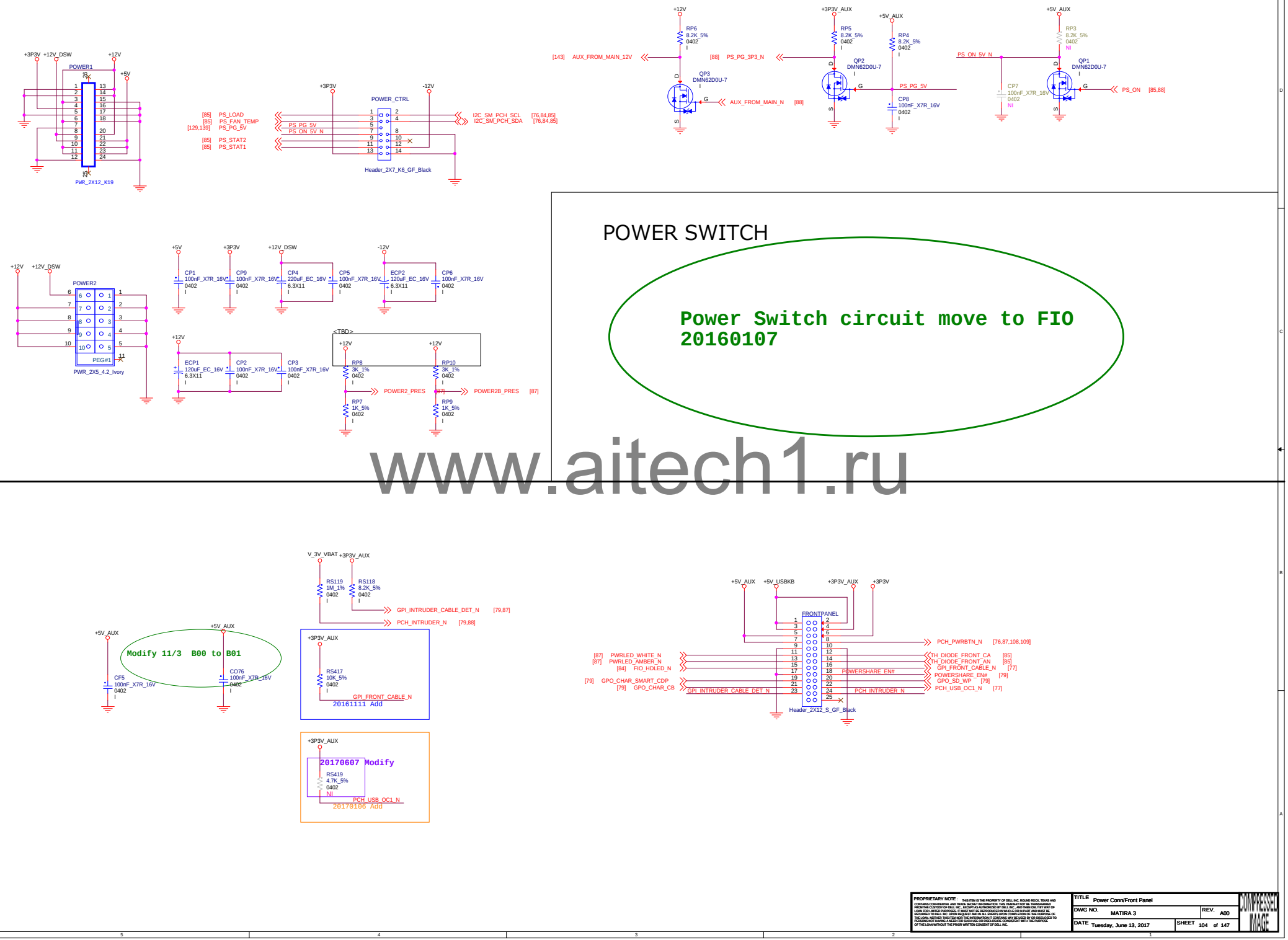
J-COMPRESSED IMAGE

POWER1 Connector



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	DWG NO. MATIRA 3	REV. A00	
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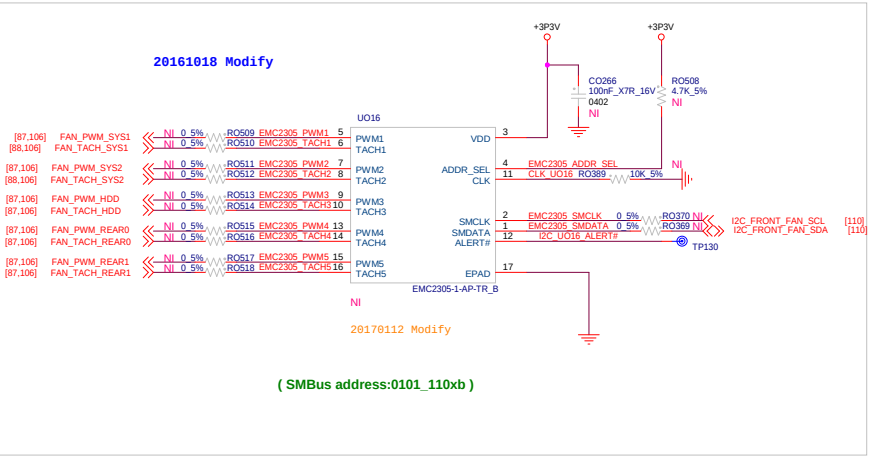
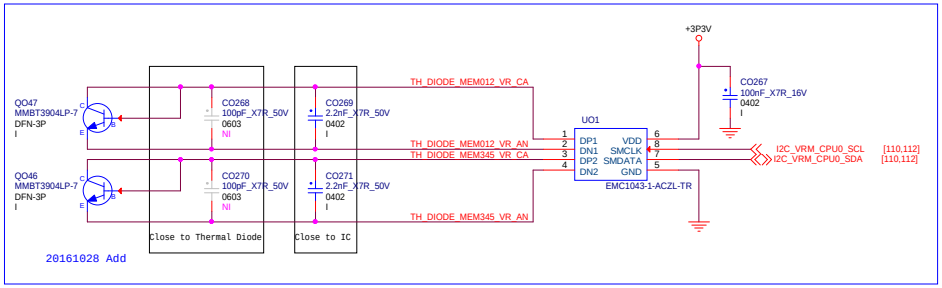
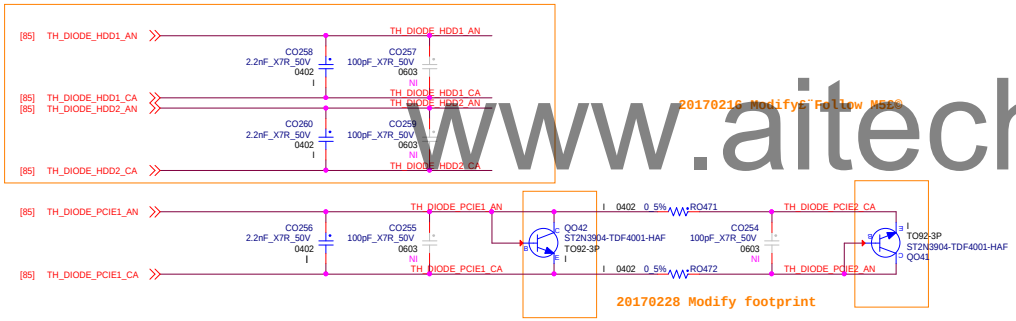
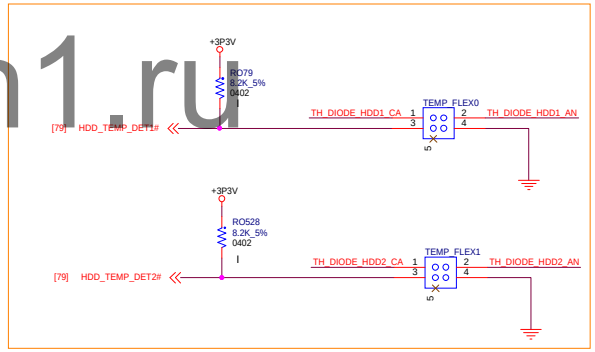
CPU/MEM VR AND AMBIENT THERMAL SENSOR









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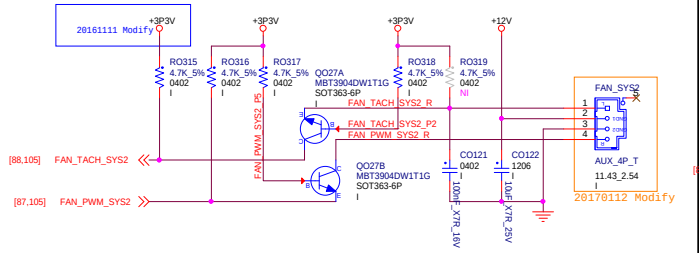
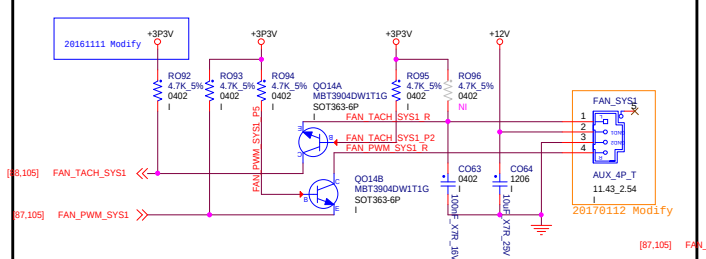
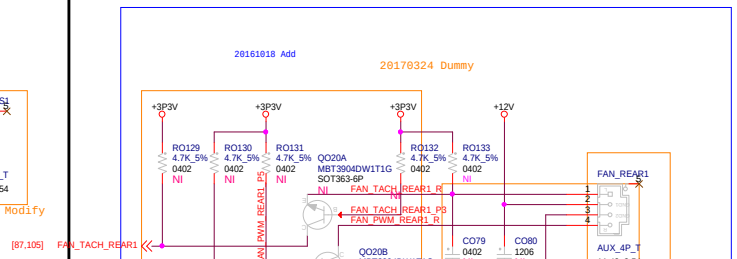
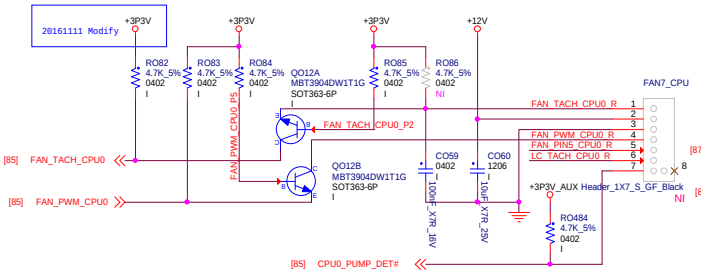
	DWG NO. MATIRA 3	REV. A00	
	DATE Tuesday, June 13, 2017	SHEET 105 of 147	

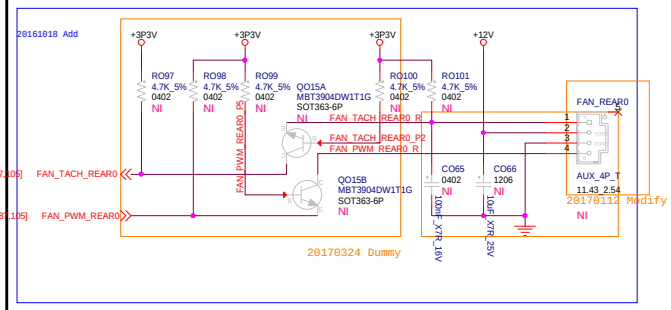
COMPRESSED IMAGE



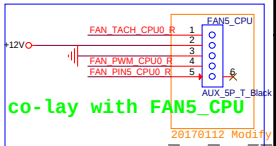




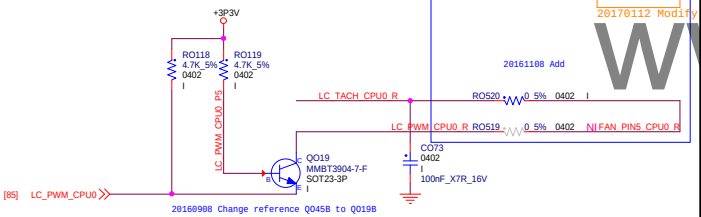


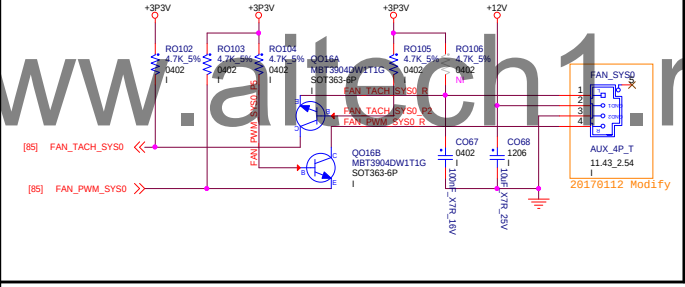


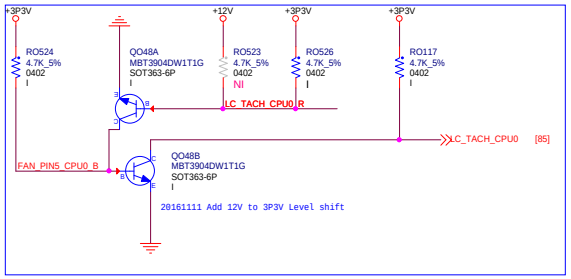
FAN 5Pin	RO520 Install RO519 Non-install (Default)	Compatible with Avalon3,PUMP can be monitored and indirectly detected,but not controlled
FAN 7Pin	RO520 Non-install RO519 Install	Not compatible with Avalon3,PUMP can be monitored,detected and controlled



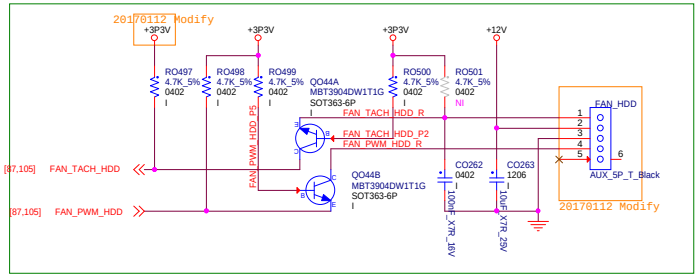
FAN7_CPU co-lay with FAN5_CPU







20160726 Add



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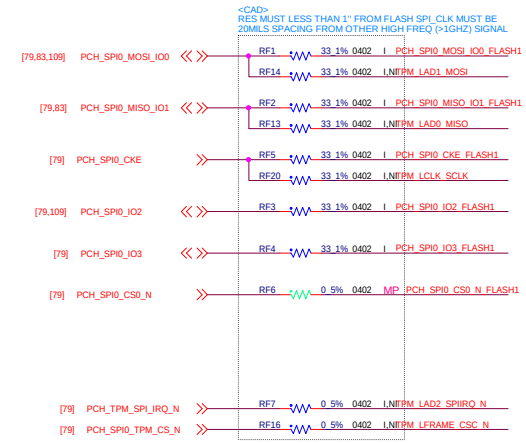
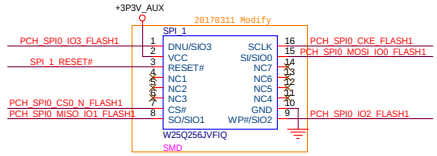
TITLE	Fan Conector		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	106 of 147

COMPRESSED IMAGE

SPI FLASH ROM

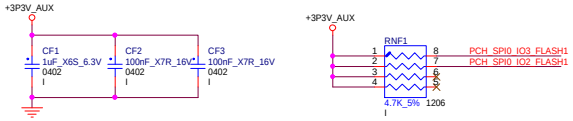




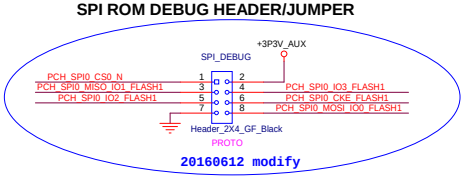
20170505 Modify

@SPI_1

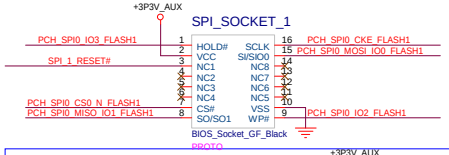
@SPI_1



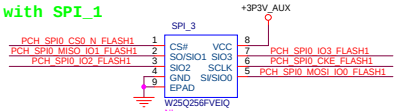
SPI ROM DEBUG HEADER/JUMPER



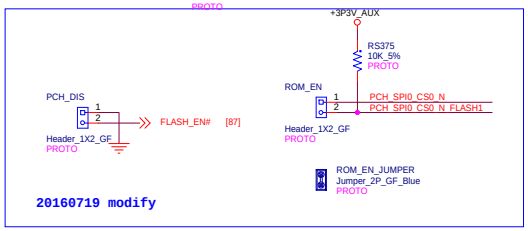
20160612 modify



SPI_3 co-lay with SPI_1



20160721 Update SPI_3 library



20160719 modify

SPI ROM Truth Table

PCH_DIS	ROM_EN	Function
Open	Install	Onboard ROM boot
Open	Open	SPI Emulator Boot
Install	Open	No boot
Install	Install	DediProg update Onboard ROM

TPM2.0 No support TCM

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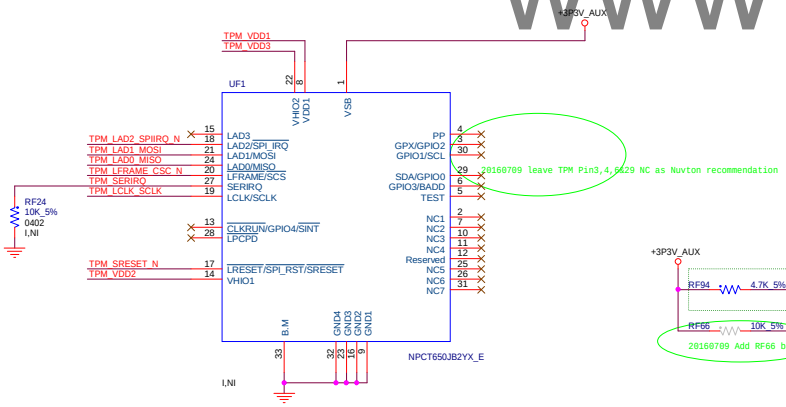
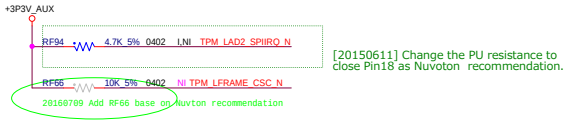
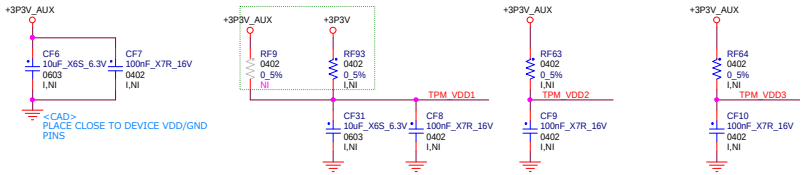
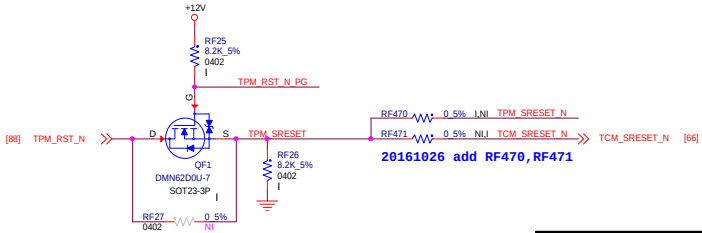




[20150611] Change the PU resistance to close Pin18 as Nuvoton recommendation.

[20150611] Reserve PU to +3P3V for TPM_VDD1 as Nuvoton recommendation.
[20150615] Populate RF93 and de-populate RF9 and add CF31 as Nuvoton recommendation.





20161026 add RF470,RF471

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TITLE	TPM/SPI		
DWG NO.	MATIRA 3	REV.	A00
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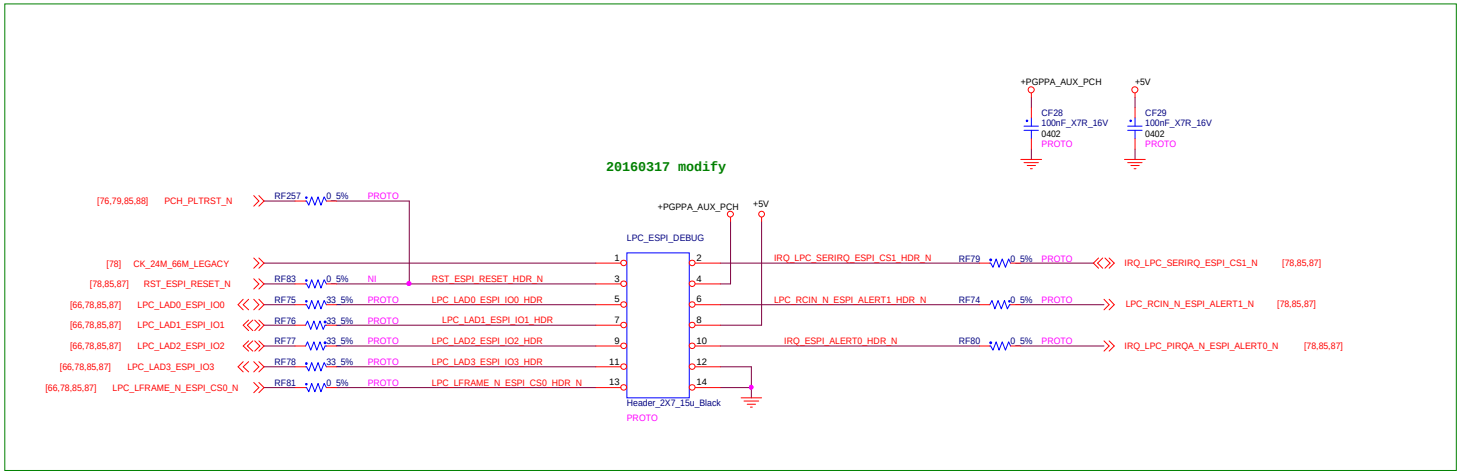
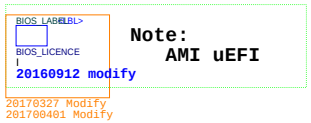
COMPRESSED IMAGE

LPC/ESPI DEBUG HEADER



Licence Label



Note:
AMI uEFI

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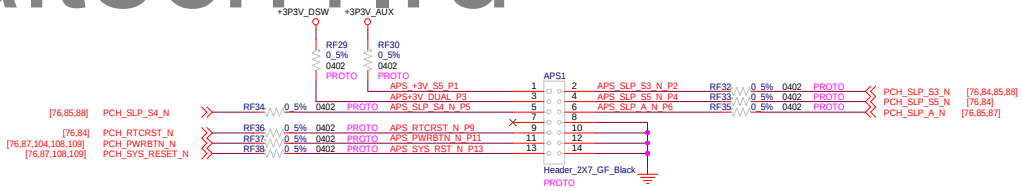
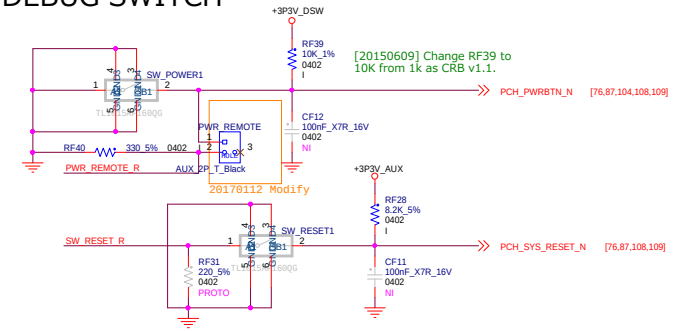
APS HEADER

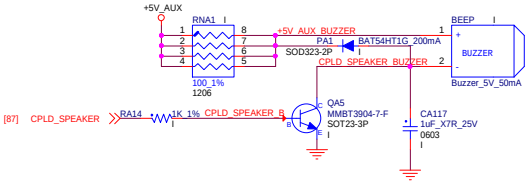


DEBUG SWITCH



BUZZER

20160921 Modify



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TITLE	Debug/Label/Misc		
DWG NO.	MATIRA 3	REV.	A00
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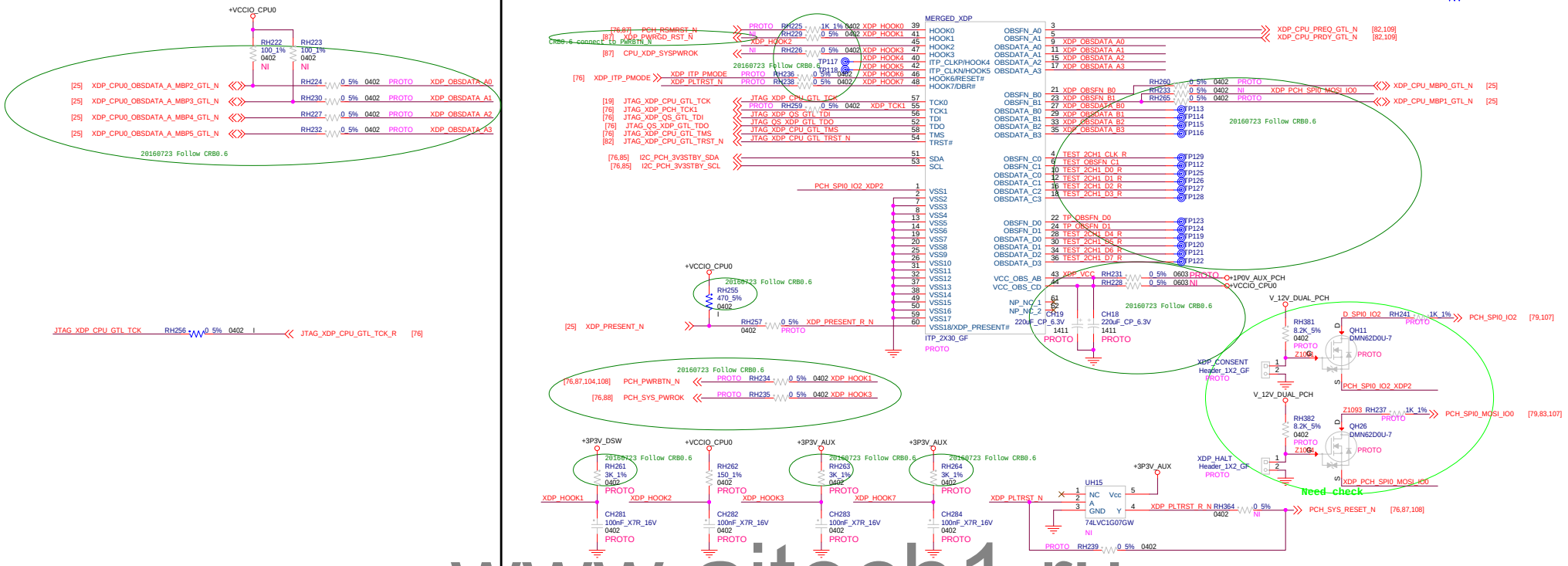
COMPRESSED IMAGE

MERGED XDP - DCI



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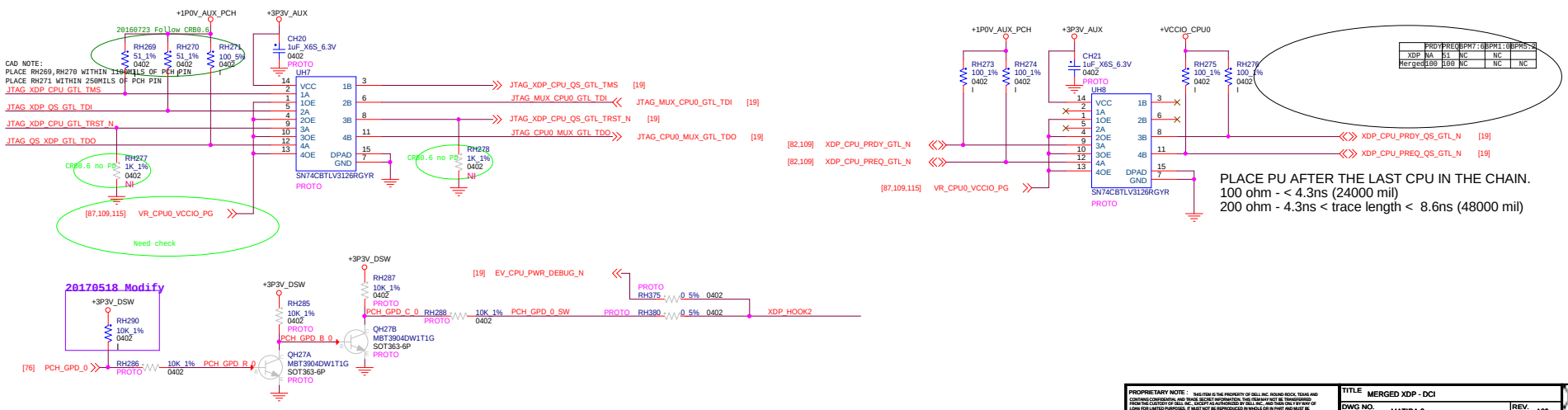

	PRDY	PREQ	BPM7:6	BPM1:0	BPM5:2
XDP	NA	51	NC	NC	
Merged	100	100	NC	NC	NC

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TITLE	MERGED XDP - DCI		
DWG NO.	MATIRA 3	REV.	A00
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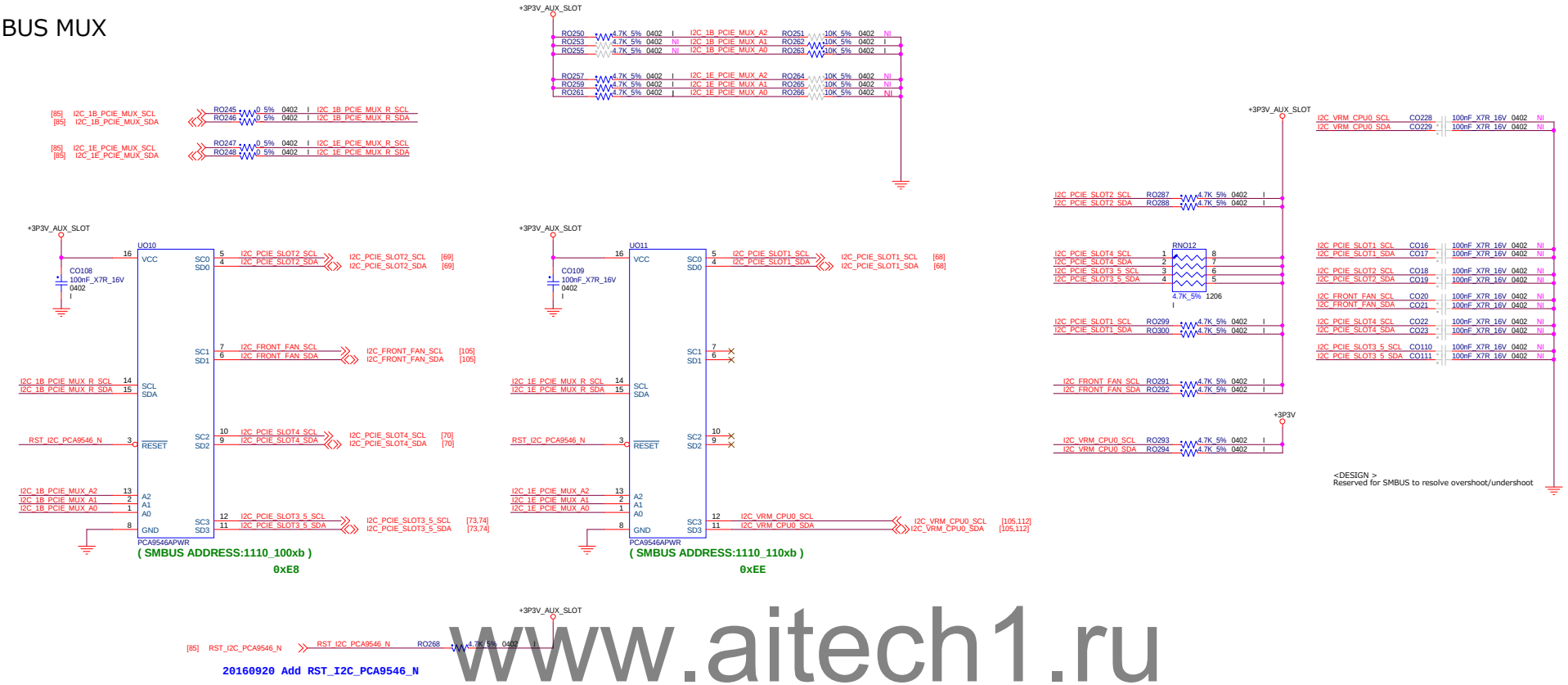
UNCLASSIFIED IMAGE

SMBUS MUX



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TITLE	SMBUS MUX		
DWG NO.	MATIRA 3	REV.	A00
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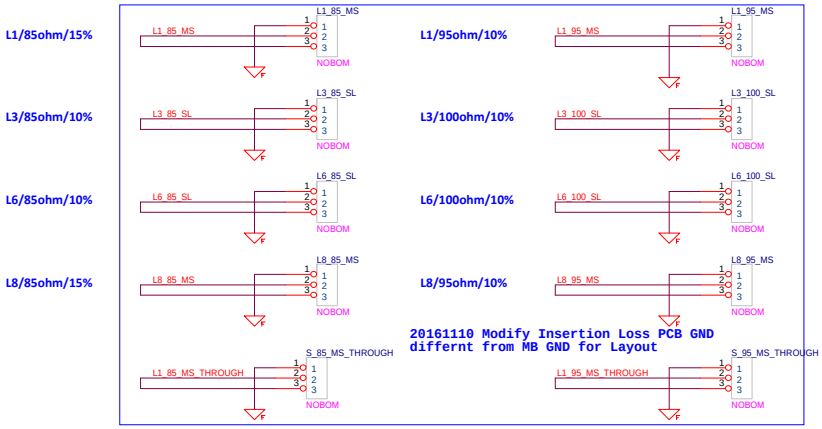
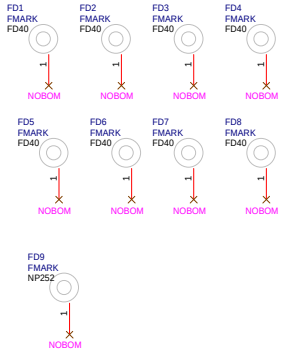
UNCLASSIFIED IMAGE

Insertion Loss Measurement

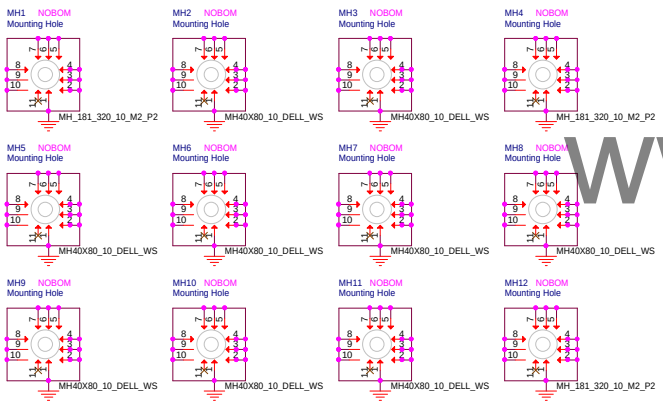


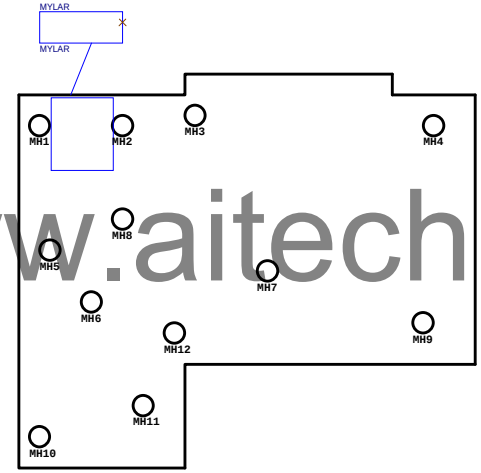
Impedance Control Test Coupon

MTG Holes



MOUNTING HOLES





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TITLE	OTHER		
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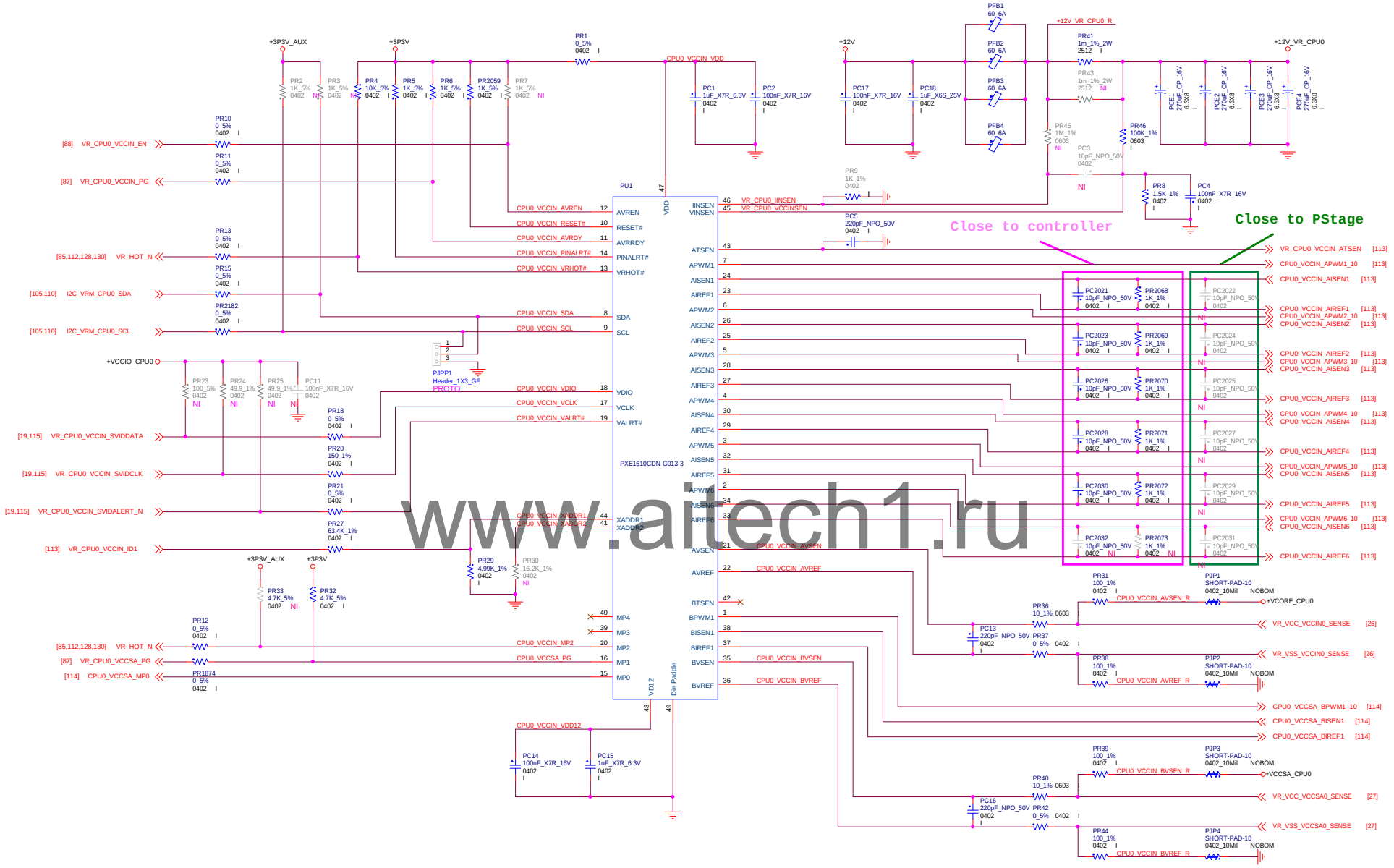
COMPRESSED IMAGE

+VCORE_CPU0_Controller

VCCIN/SA SVID Address:0,1
PMBus Address:0xC0



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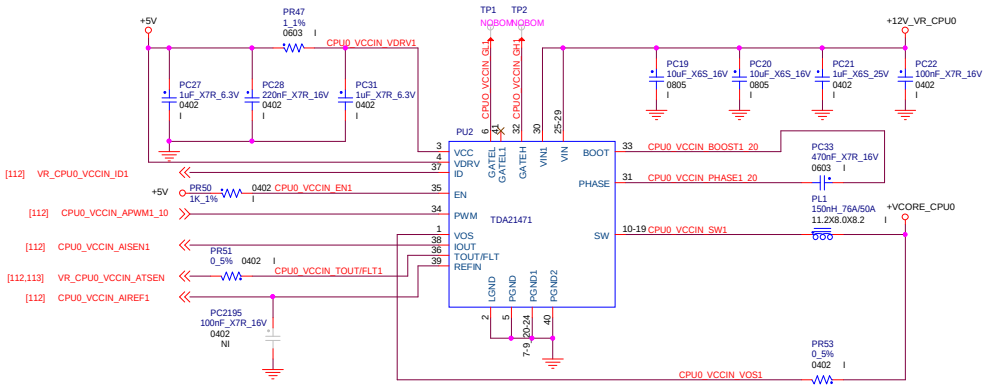
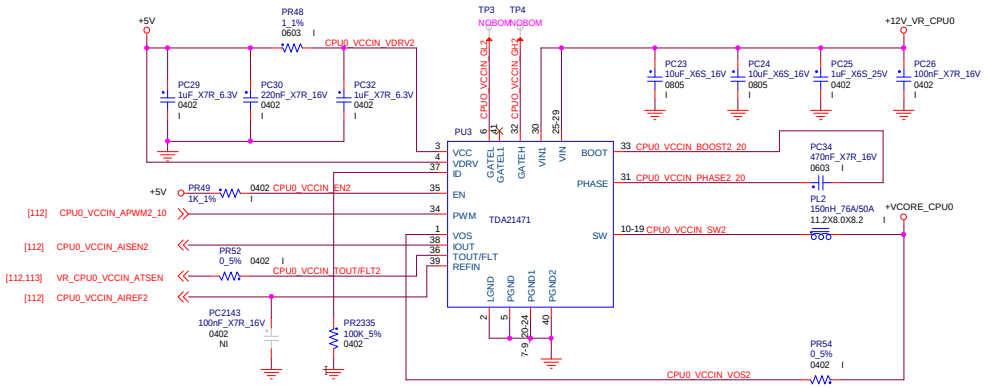
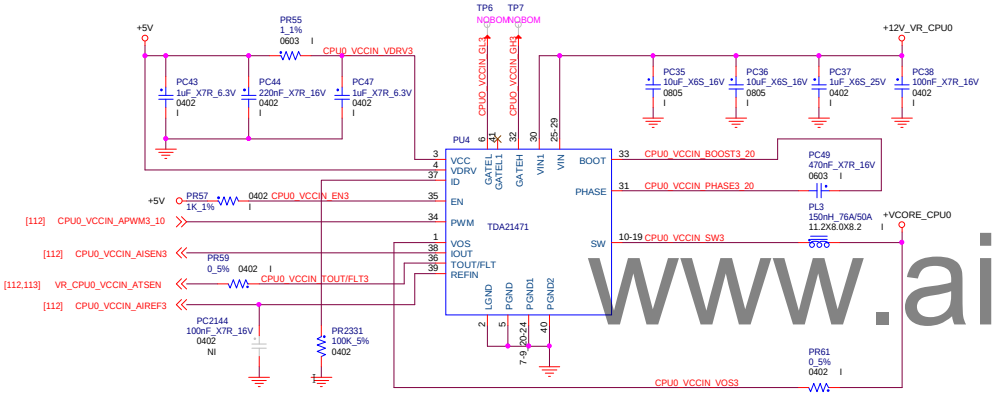
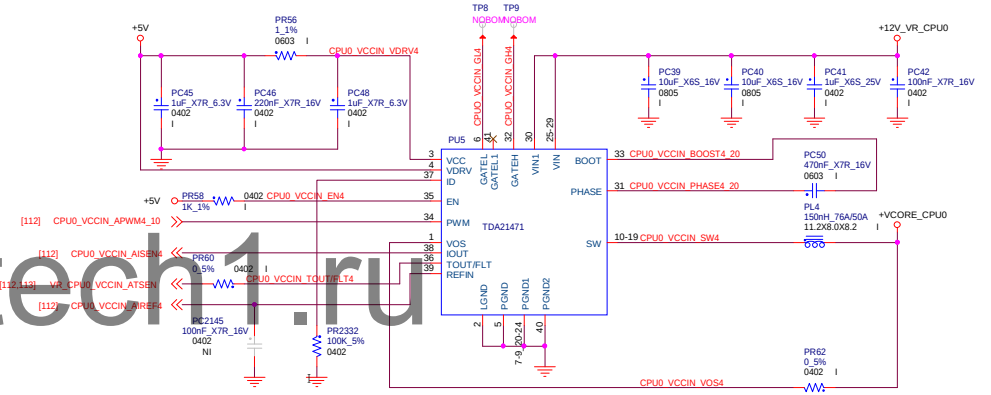
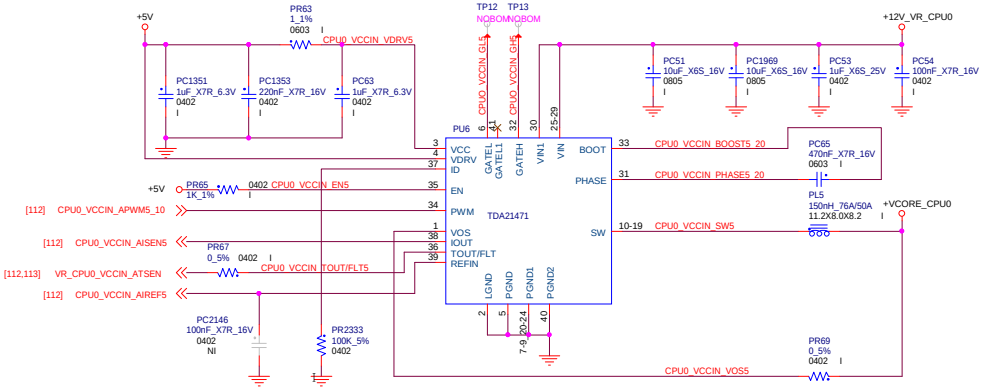
+VCORE_CPU0_Driver

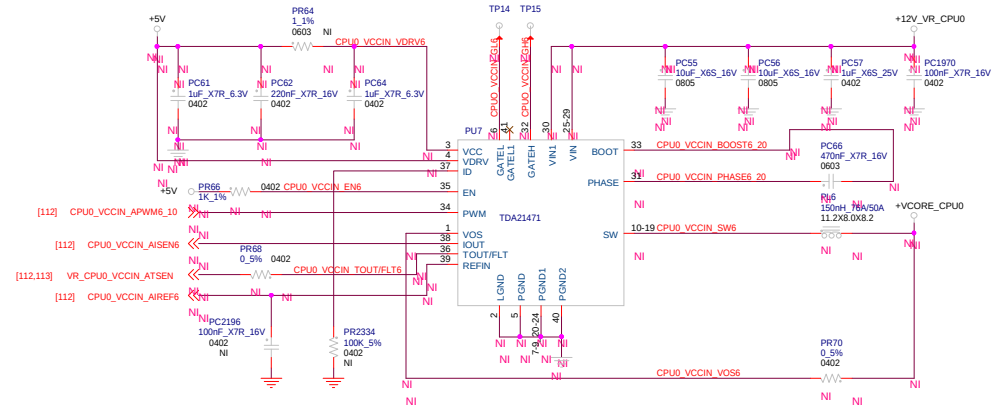












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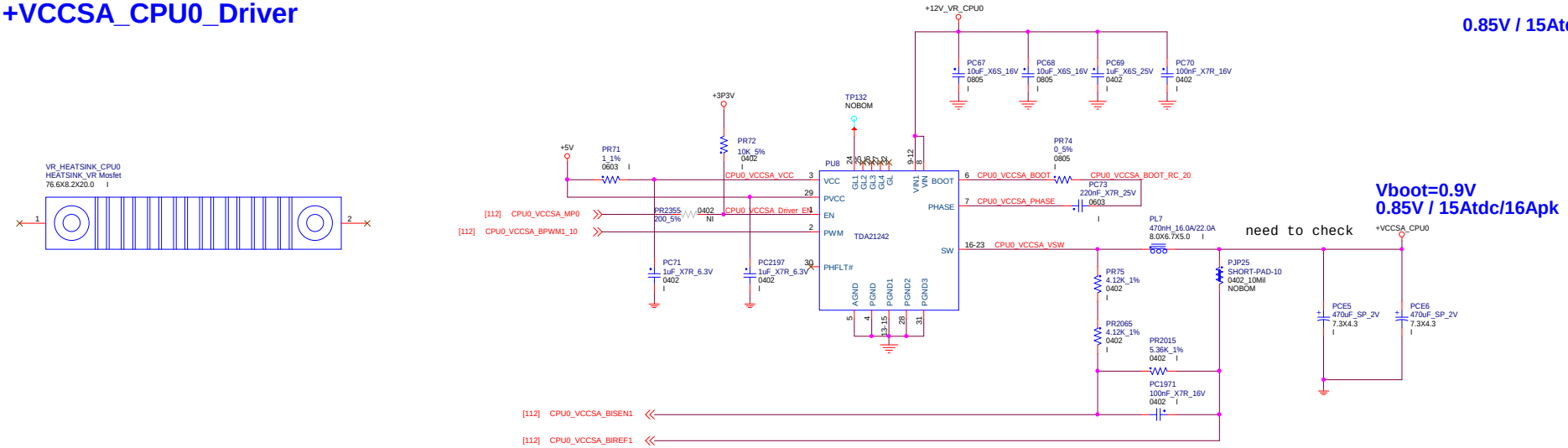
TITLE VR, CPU0 CORE DRIVER		
DWG NO. MATIRA 3	REV. A00	
DATE Tuesday, June 13, 2017	SHEET 113 of 147	

COMPRESSED IMAGE

+VCCSA_CPU0_Driver

Vboot=0.9V

0.85V / 15Atdc/16Apk

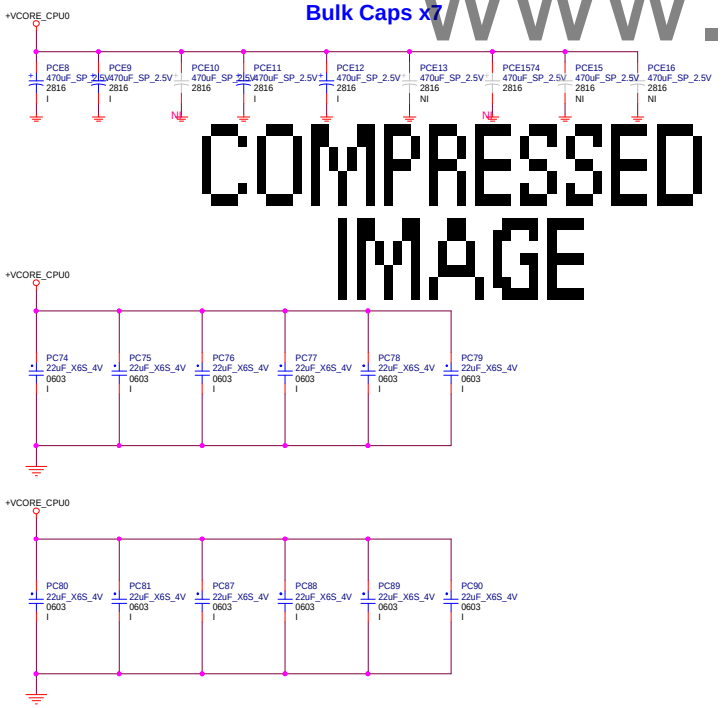


Vboot=0.9V
0.85V / 15Atdc/16Apk

CPU0 VCCIN CAP

+1.8V / 89Atdc/228Apk
Vboot=1.7V

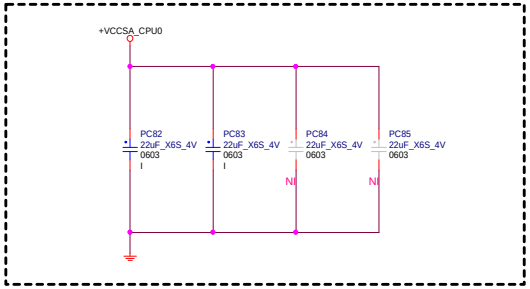
Bulk Caps x7



COMPRESSED IMAGE

CPU0 VCCSA CAP

Place 4 VR output inductor



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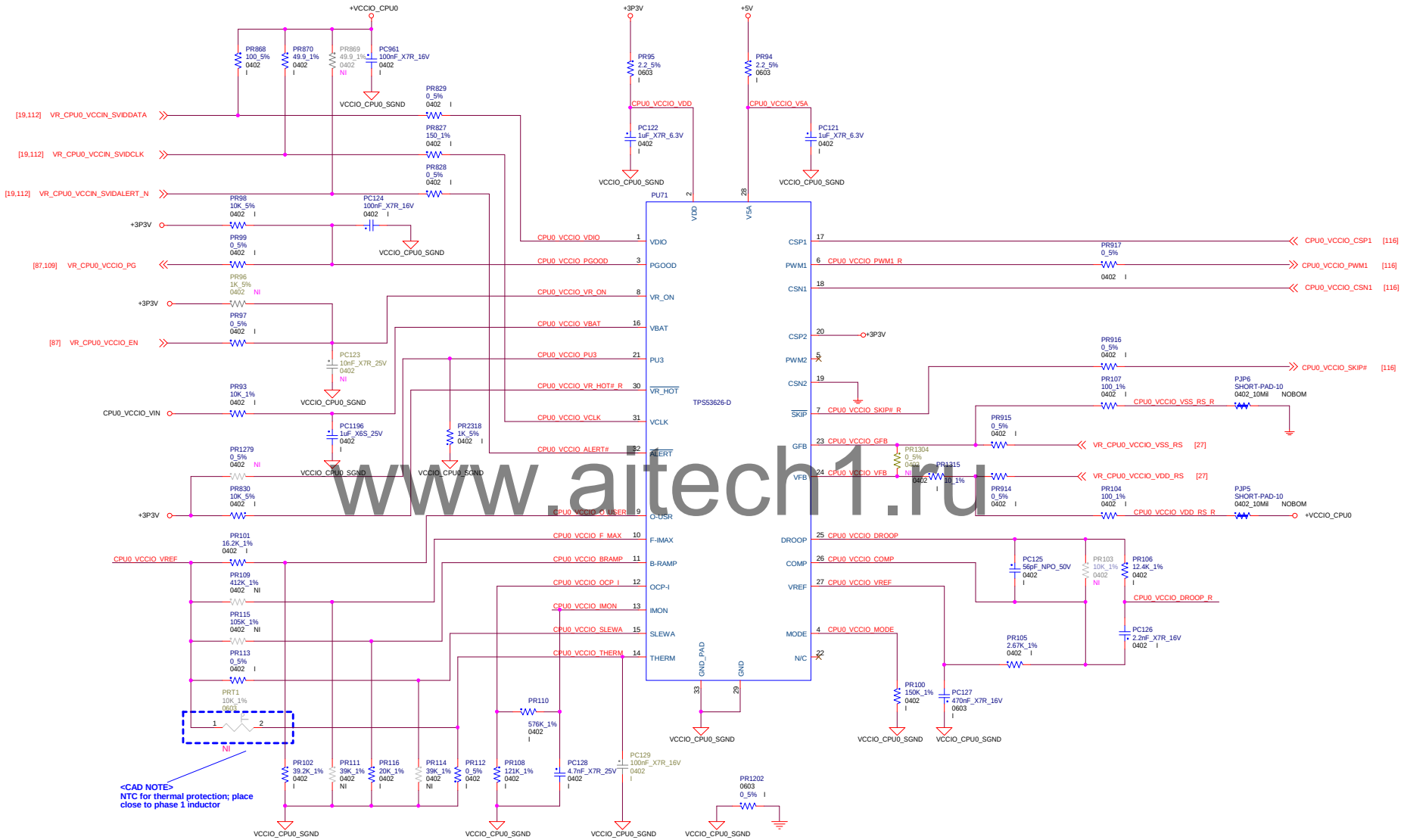
TITLE VR, CPU0 VCCSA DRIVER		
DWG NO. MATIRA 3	REV. A00	
DATE Tuesday, June 13, 2017	SHEET 114 of 147	

COMPRESSED IMAGE

+VCCIO_CPU0_Controller

CPU0
VCCIO SVID Bus= 02h



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TITLE	VR, CPU0 VCCIO CONTROLLER
DWG NO.	MATIRA 3
REV.	A00
DATE	Tuesday, June 13, 2017
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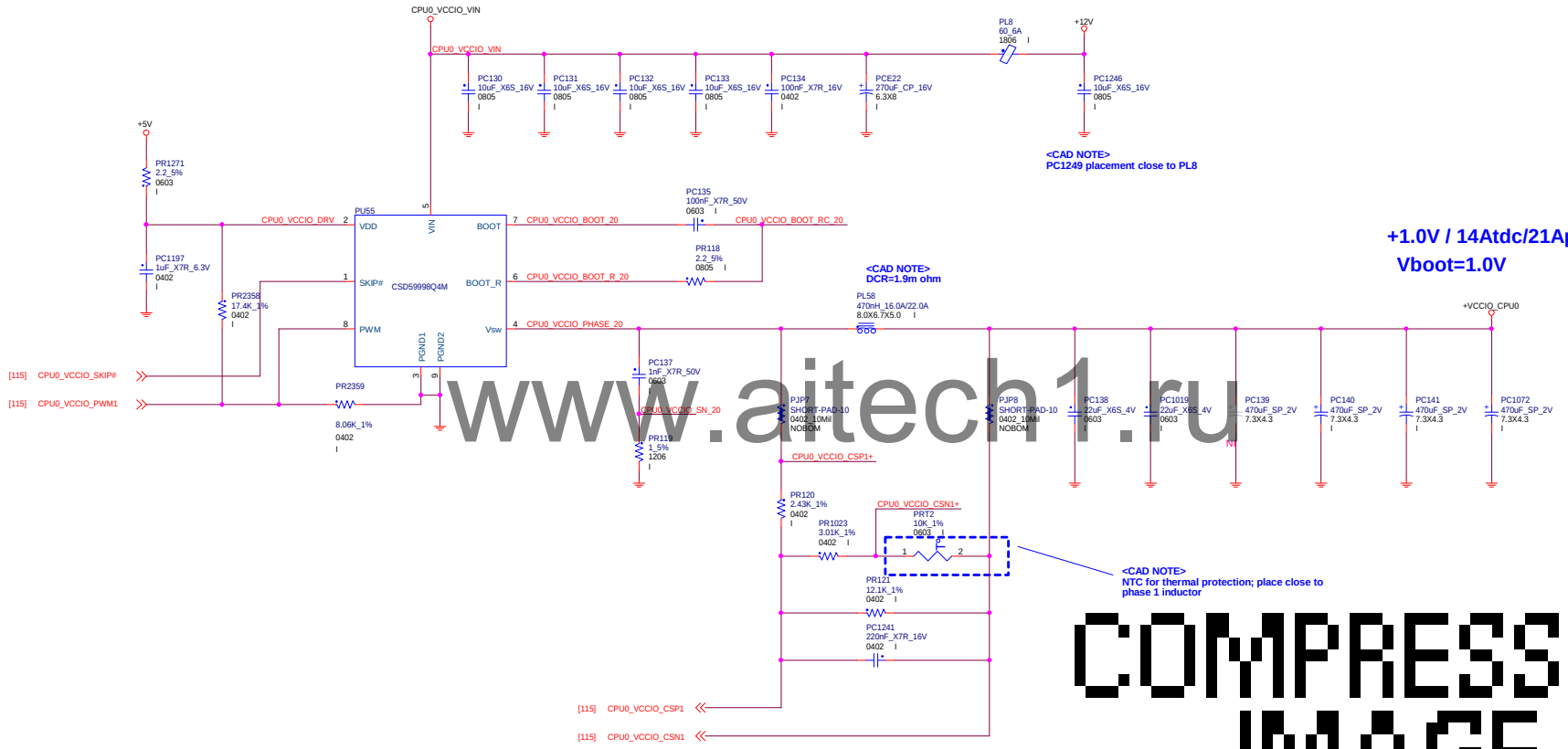
+VCCIO_CPU0_DRIVER



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TITLE	VR, CPU0 VCCIO DRIVER		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	116 of 147

COMPRESSED IMAGE

+VMCP_CPU0_Controller (EMPTY)

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TITLE VR, CPU0 VMCP CONTROLLER (EMPTY)		
DWG NO. MATIRA 3	REV. A00	
DATE Tuesday, June 13, 2017	SHEET 117 of 147	

COMPRESSED IMAGE

+VMCP_CPU0_DRIVER(EMPTY)

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TITLE	VR, CPU0 VMCP DRIVER (EMPTY)	
DWG NO. MATIRA 3		REV. A00
DATE Tuesday, June 13, 2017	SHEET 118 of 147	

COMPRESSED IMAGE

+1V0_CPU0_Controller

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TITLE	VR. CPU0 1V0 CONTROLLER (EMPTY)		
DWG NO.	MATIRA 3	REV.	A00
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TITLE	VR, CPU1 CORE CONTROLLER (EMPTY)		
DWG NO.	MATIRA 3	REV.	A00
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TITLE	VR, CPU1 CORE DRIVER (EMPTY)		
DWG NO.	MATIRA 3	REV.	A00
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TITLE	VR, CPU1 VCCSA DRIVER (EMPTY)		
DWG NO.	MATIRA 3	REV.	A00
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TITLE	VR, CPU1 VCCIO CONTROLLER (EMPTY)		
DWG NO.	MATIRA 3	REV.	A00
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TITLE	VR, CPU1 VCCIO DRIVER (EMPTY)		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	124 of 147

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TITLE	VR, CPU1 VMCP CONTROLLER (EMPTY)		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	125 of 147

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TITLE	VR, CPU1 VMCP DRIVER (EMPTY)		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	126 of 147

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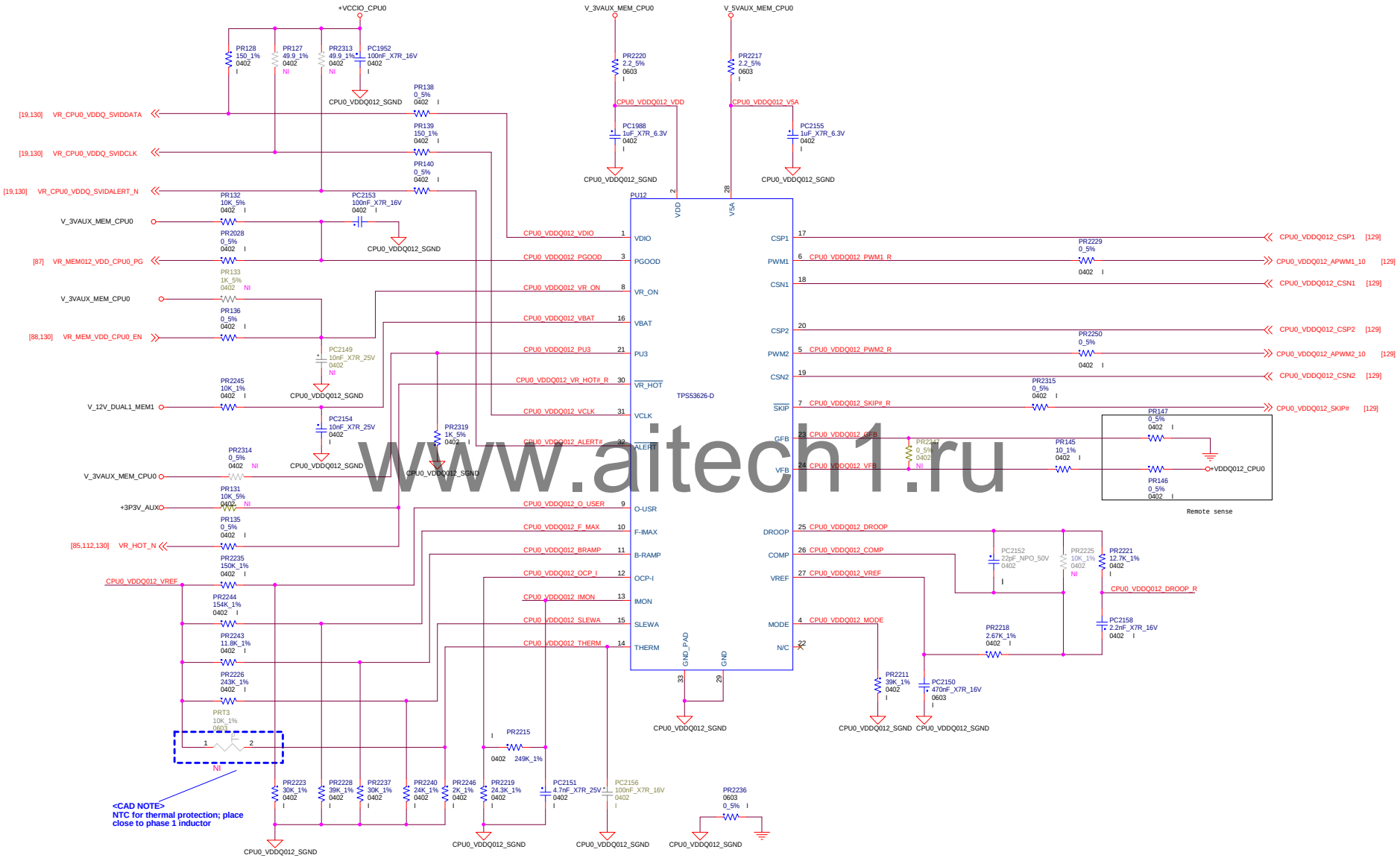
TITLE	VR. CPU1 1V0 CONTROLLER (EMPTY)		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	127 of 147

COMPRESSED IMAGE

+VDDQ012_CPU0_Controller



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TITLE	VR, CPU0 DDR012 CONTROLLER
DWG NO.	MATIRA 3
REV.	A00
DATE	Tuesday, June 13, 2017
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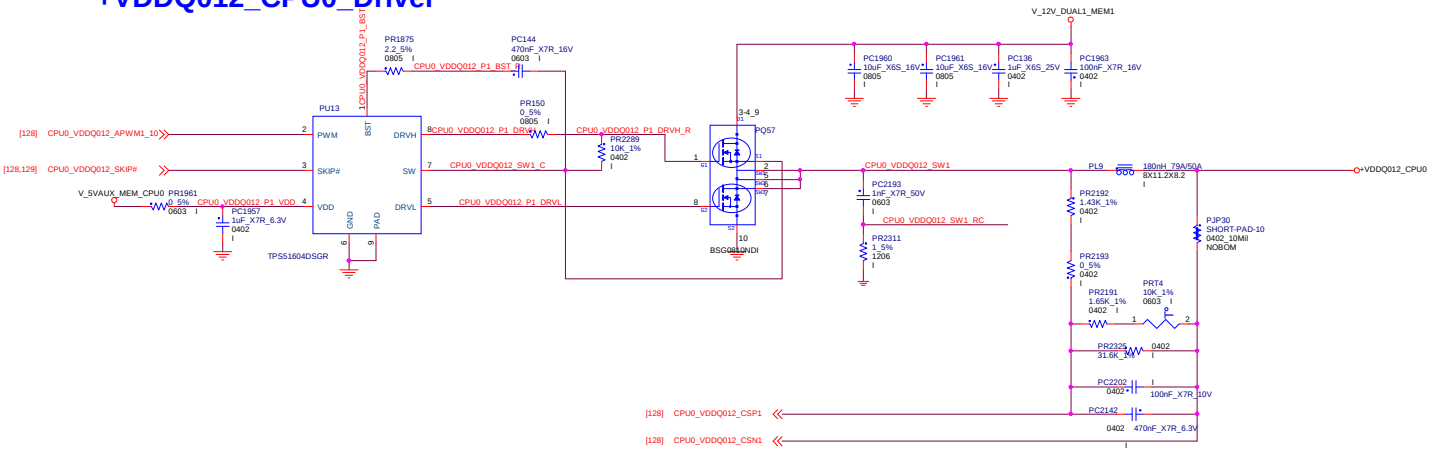
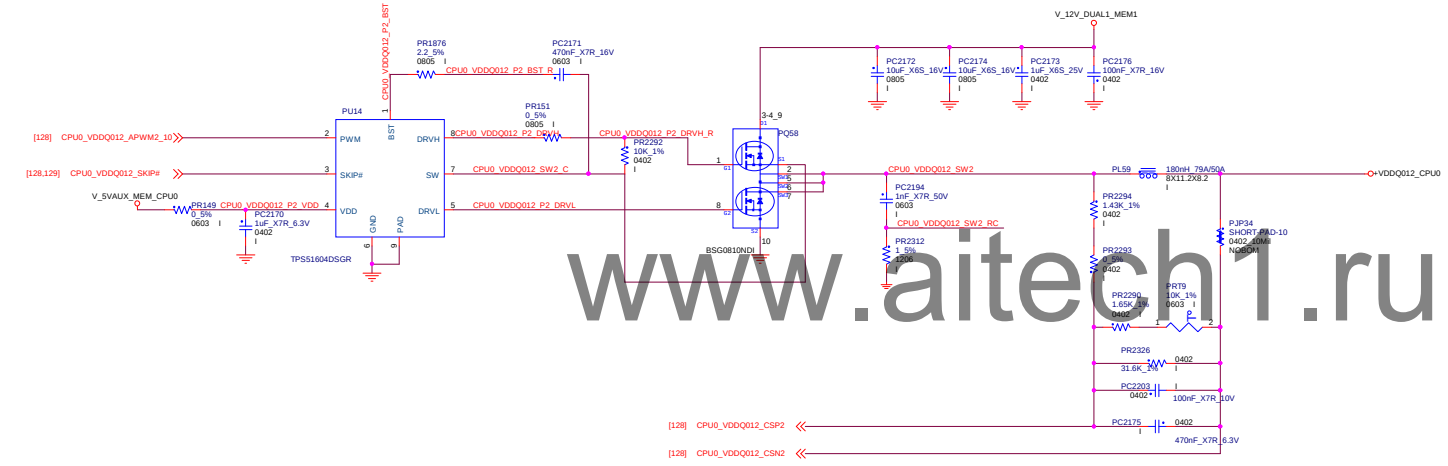
COMPRESSED IMAGE

+VDDQ012_CPU0_Driver





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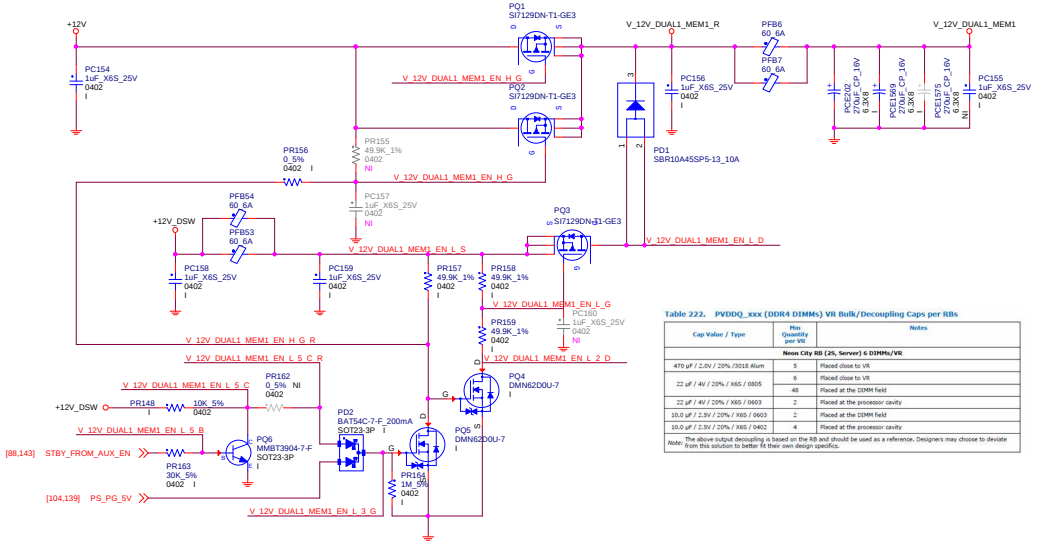
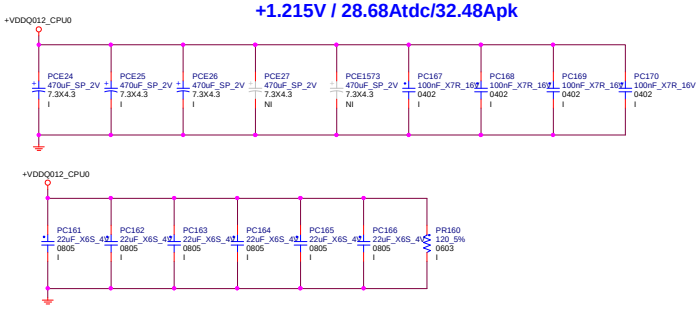


Table 222. PVDDQ_xxx (DDR4 DIMMs) VR Bulk/Decoupling Caps per RBs

Cap Value / Type	Min Quantity per VR	Notes
Neon City RB (2S, Server) 6 DIMMs/VR		
470 µF / 2.0V / 20% /3018 Alum	5	Placed close to VR
22 µF / 4V / 20% / X6S / 0805	6	Placed close to VR
	48	Placed at the DIMM field
22 µF / 4V / 20% / X6S / 0603	2	Placed at the processor cavity
10.0 µF / 2.5V / 20% / X6S / 0603	2	Placed at the DIMM field
10.0 µF / 2.5V / 20% / X6S / 0402	4	Placed at the processor cavity

Note: The above output decoupling is based on the RB and should be used as a reference. Designers may choose to deviate from this solution to better fit their own design specifics.

+1.215V / 28.68Atdc/32.48Apk



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TITLE	VR, CPU0 VDDQ012 DRIVER
DWG NO.	MATIRA 3
REV.	A00
DATE	Tuesday, June 13, 2017
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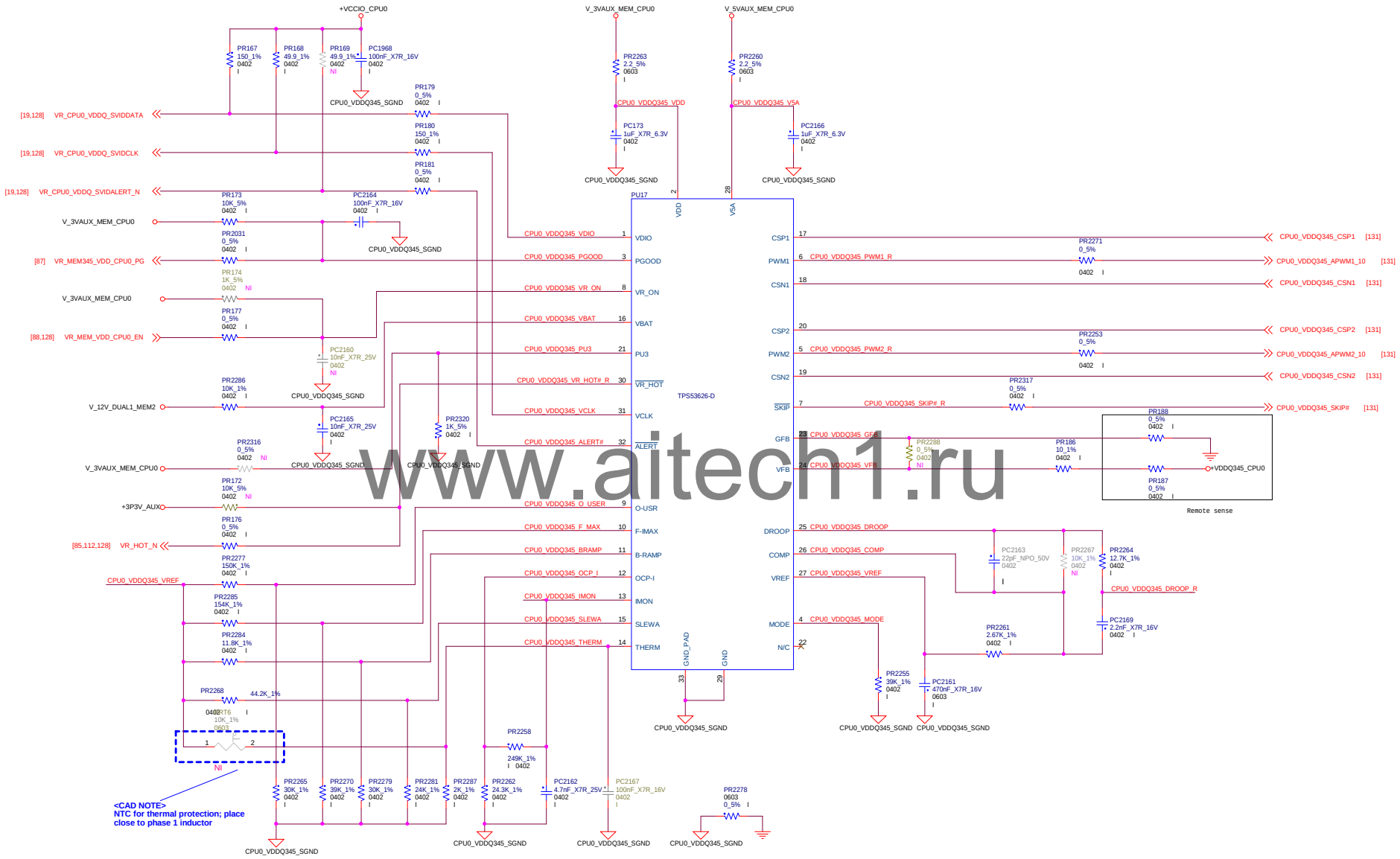
COMPOSITE IMAGE

+VDDQ345_CPU0_Controller



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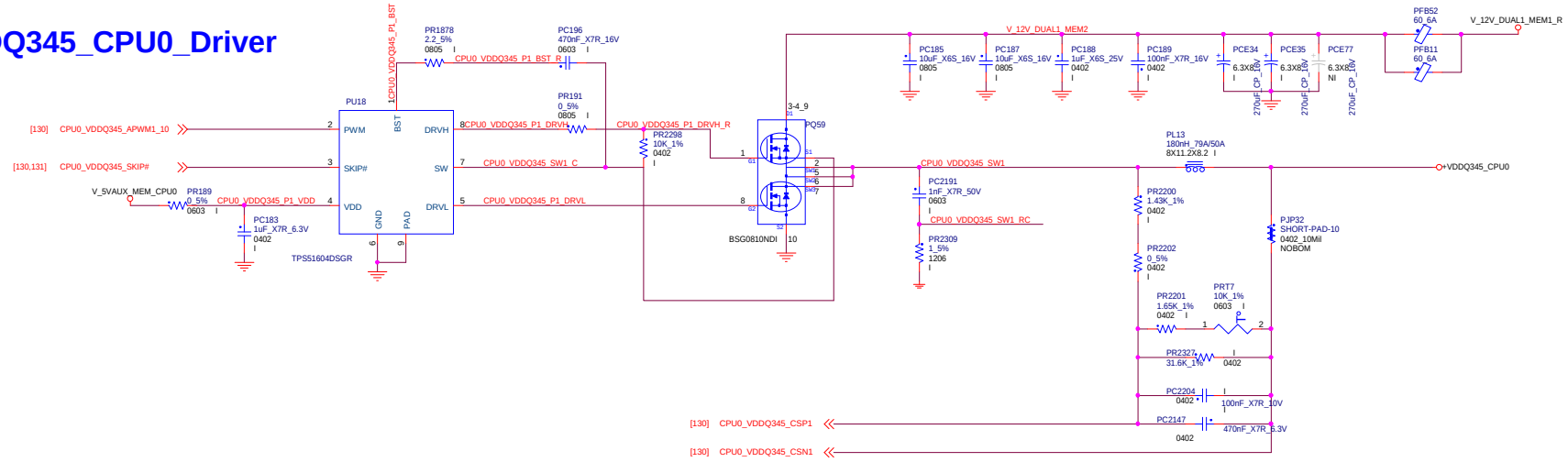
TITLE	VR, CPU0 VDDQ345 CONTROLLER		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	130 of 147

COMPRESSED IMAGE

+VDDQ345_CPU0_Driver



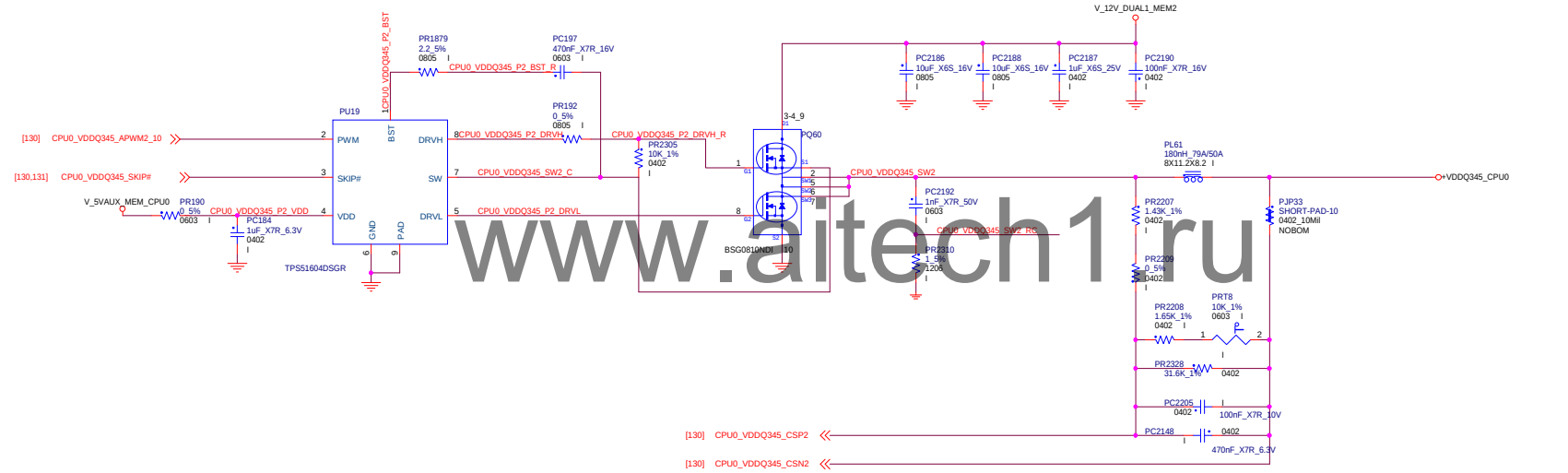


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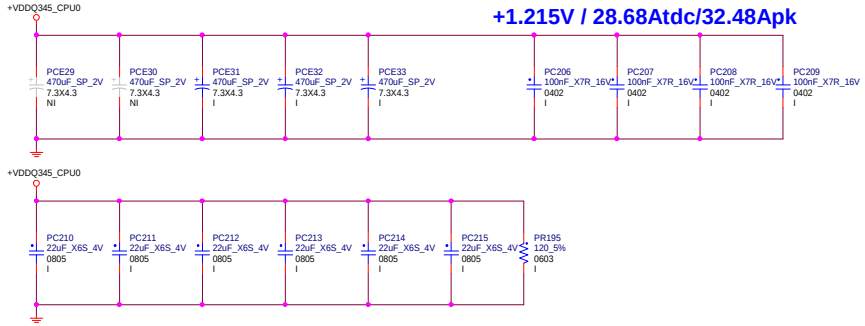
Table 222. PVDDQ_xxx (DDR4 DIMMs) VR Bulk/Decoupling Caps per RBs

Cap Value / Type	Min Quantity per VR	Notes
Neon City RB (2S, Server) 6 DIMMs/VR		
470 µF / 2.0V / 20% /3018 Alum	5	Placed close to VR
22 µF / 4V / 20% / X6S / 0805	6	Placed close to VR
	48	Placed at the DIMM field
22 µF / 4V / 20% / X6S / 0603	2	Placed at the processor cavity
10.0 µF / 2.5V / 20% / X6S / 0603	2	Placed at the DIMM field
10.0 µF / 2.5V / 20% / X6S / 0402	4	Placed at the processor cavity

Note: The above output decoupling is based on the RB and should be used as a reference. Designers may choose to deviate from this solution to better fit their own design specifics.



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TITLE	VR, CPU0 VDDQ345 DRIVER		
DWG NO.	MATIRA 3	REV.	A00
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TITLE	VR, CPU1 VDDQ012 CONTROLLER (EMPTY)		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	132 of 147

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TITLE	VR, CPU1 VDDQ012 DRIVER (EMPTY)		
DWG NO.	MATIRA 3	REV.	A00
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TITLE	VR, CPU1 VDDQ0345 CONTROLLER (EMPTY)		
DWG NO.	MATIRA 3	REV.	A00
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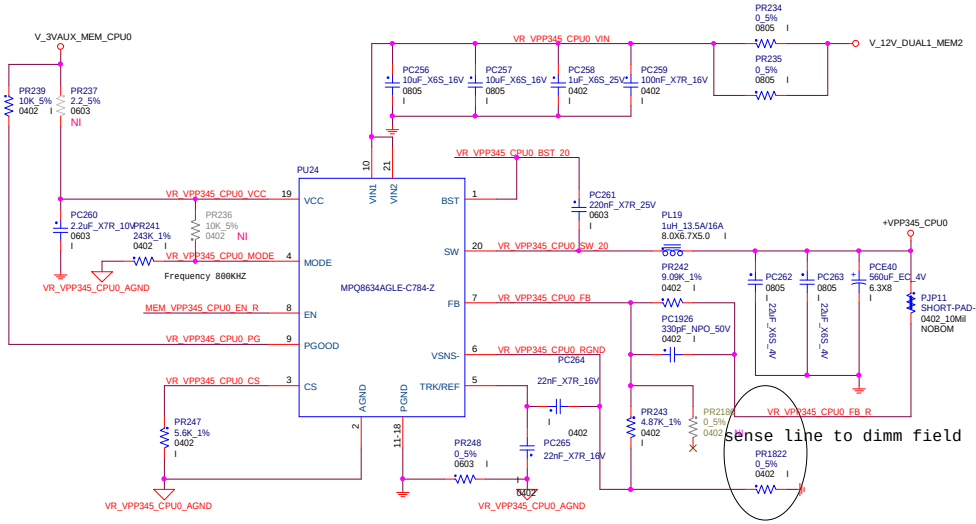
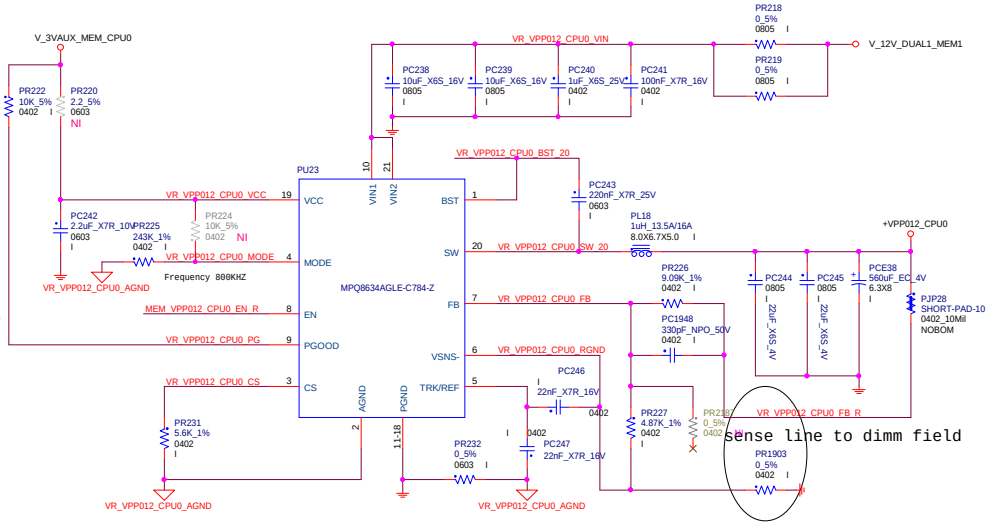
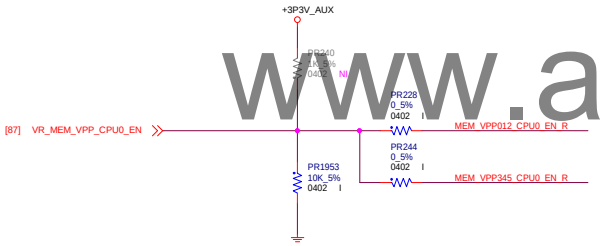
TITLE	VR, CPU1 VDDQ345 DRIVER (EMPTY)		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	135 of 147

COMPRESSED IMAGE

CPU0 MEM VPP







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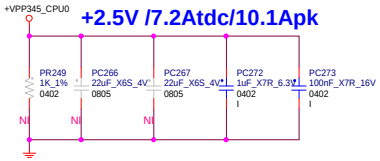

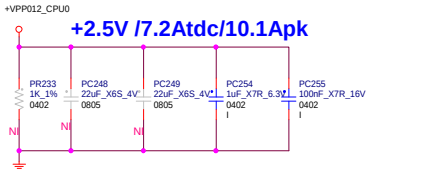

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TITLE	VR, CPU0 MEMORY VPP		
DWG NO.	MATIRA 3	REV.	A00
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TITLE	VR, CPU1 MEMORY VPP (EMPTY)		
DWG NO.	MATIRA 3	REV.	A00
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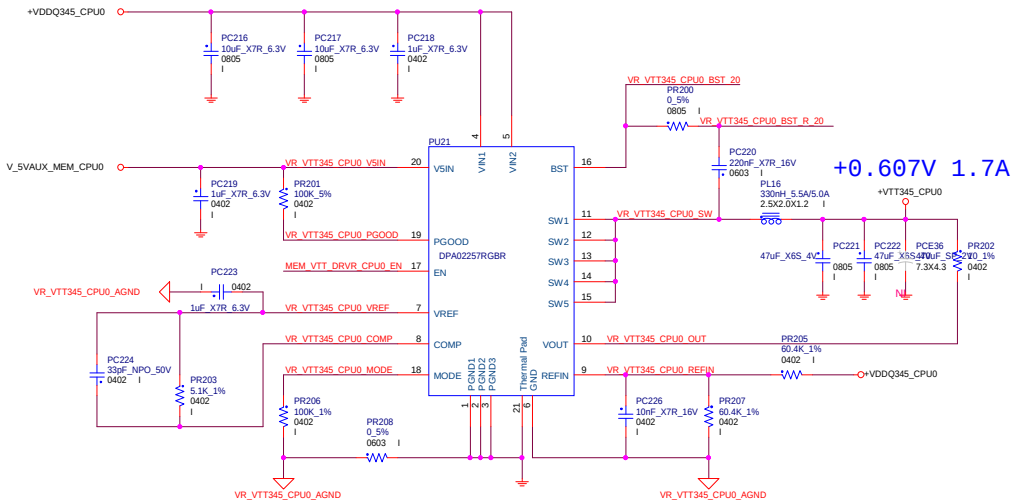
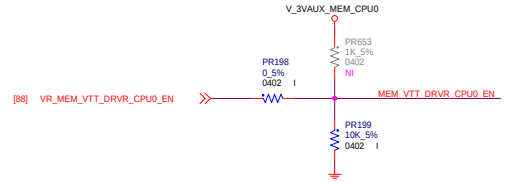
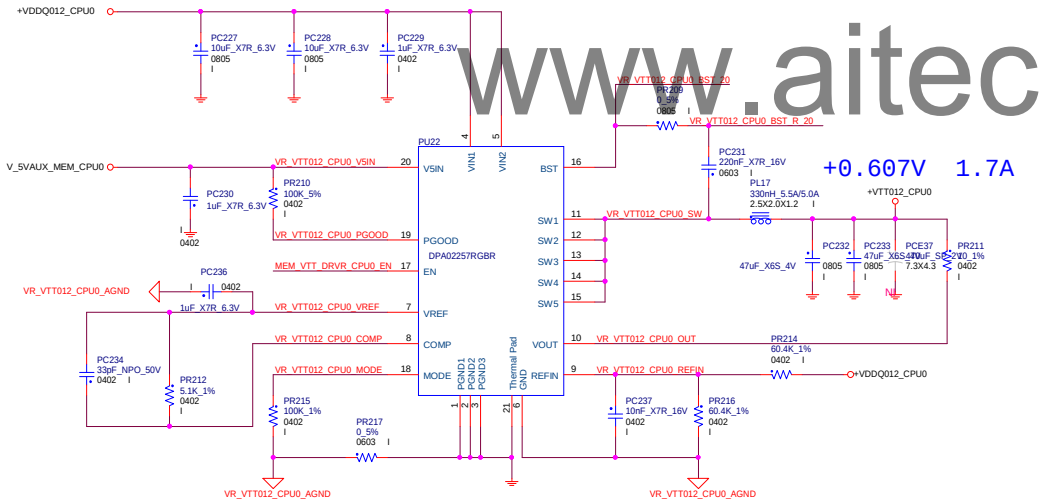
COMPRESSED IMAGE

DDR_VTT







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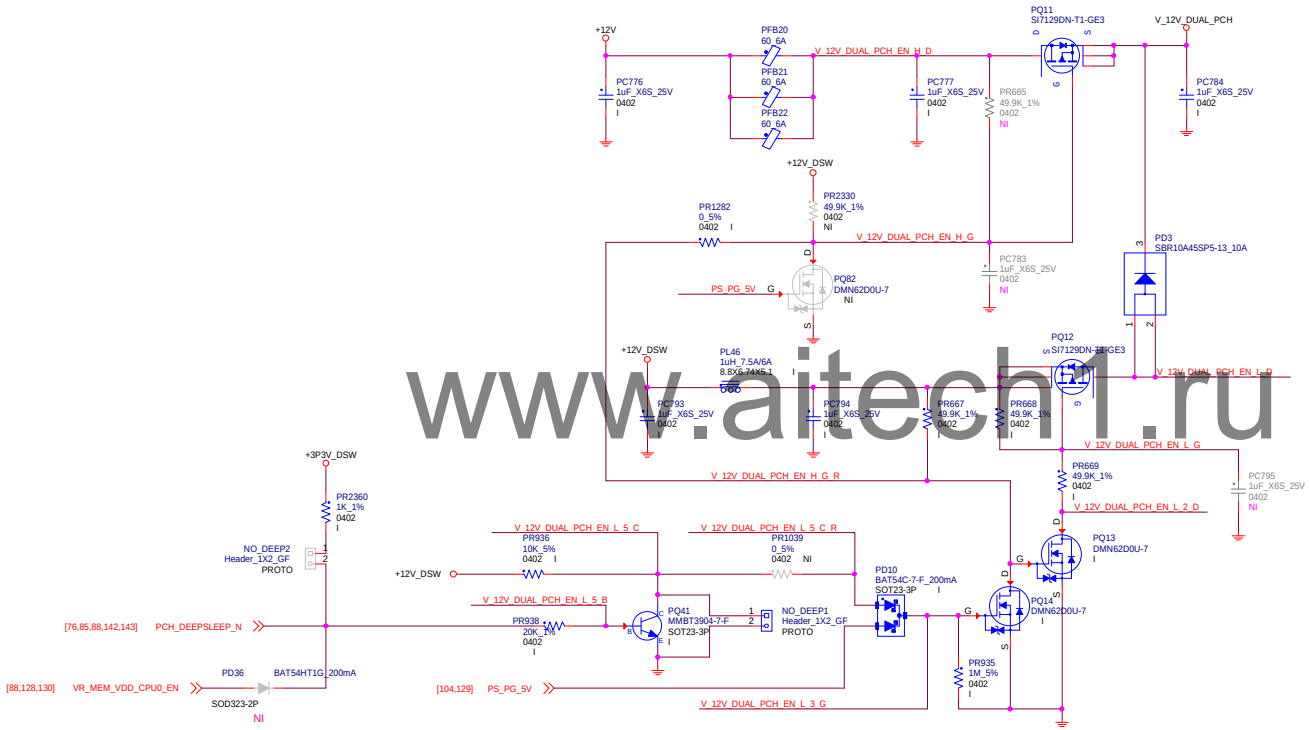
TITLE	VR, MEMORY VTT		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	138 of 147

COMPRESSED IMAGE

+12VAUX_PCH Switch



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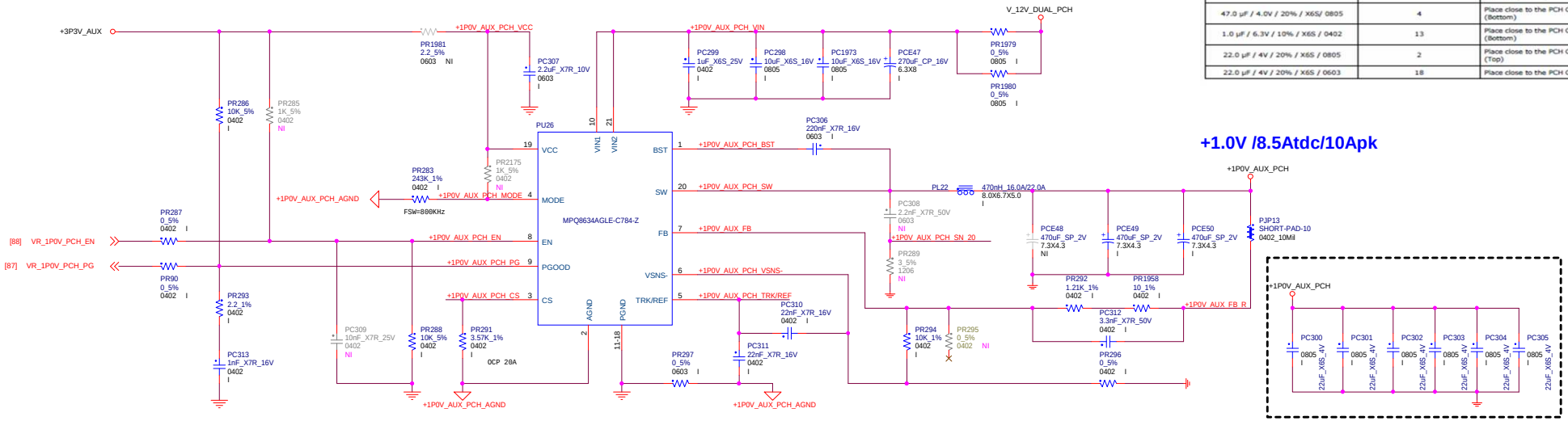
	DWG NO. MATIRA 3	REV. A00	
	DATE Tuesday, June 13, 2017	SHEET 139 of 147	

COMPRESSED IMAGE

+1P0V_AUX_PCH_Controller

P1V05_PCH_AUX VR Decoupling Caps based on Neon City RB

Cap Value	Min Quantity per VR	Notes
470. µF / 2.0V / 20% / Alum	4	bulk, place close to VR output inductor (Bottom)
47.0 µF / 4.0V / 20% / X6S/ 0805	4	Place close to the PCH Chip (Bottom)
1.0 µF / 6.3V / 10% / X6S / 0402	13	Place close to the PCH Chip (Bottom)
22.0 µF / 4V / 20% / X6S / 0805	2	Place close to the PCH Chip (Top)
22.0 µF / 4V / 20% / X6S / 0603	18	Place close to the PCH Chip



+1P8V_Controller

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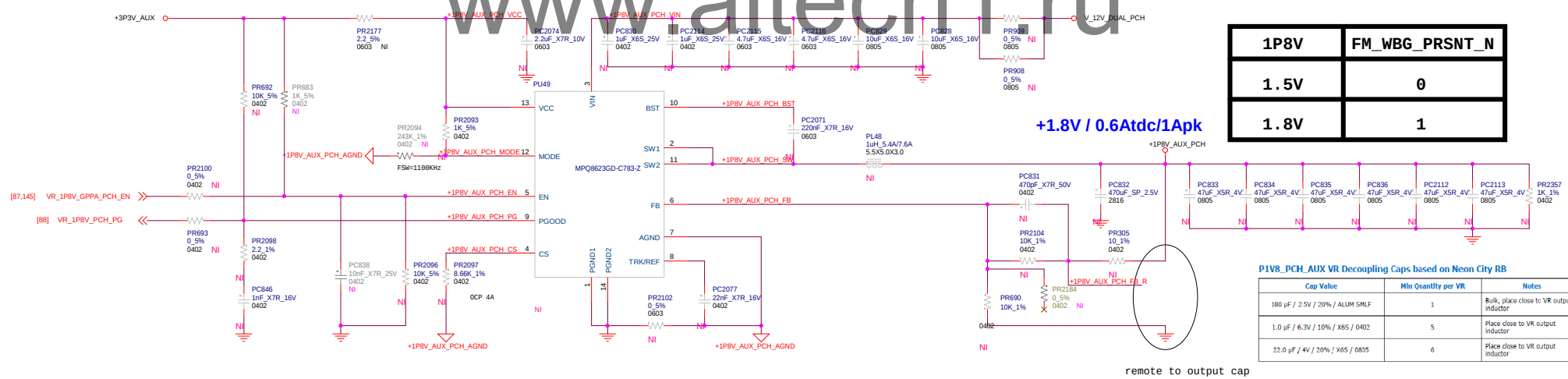
1P8V	FM_WBG_PRSNT_N
1.5V	0
1.8V	1



P1V8_PCH_AUX VR Decoupling Caps based on Neon City RB

Cap Value	Min Quantity per VR	Notes
180 µF / 2.5V / 20% / ALUM SMLF	1	Bulk, place close to VR output inductor
1.0 µF / 6.3V / 10% / X6S / 0402	5	Place close to VR output inductor
22.0 µF / 4V / 20% / X6S / 0805	6	Place close to VR output inductor

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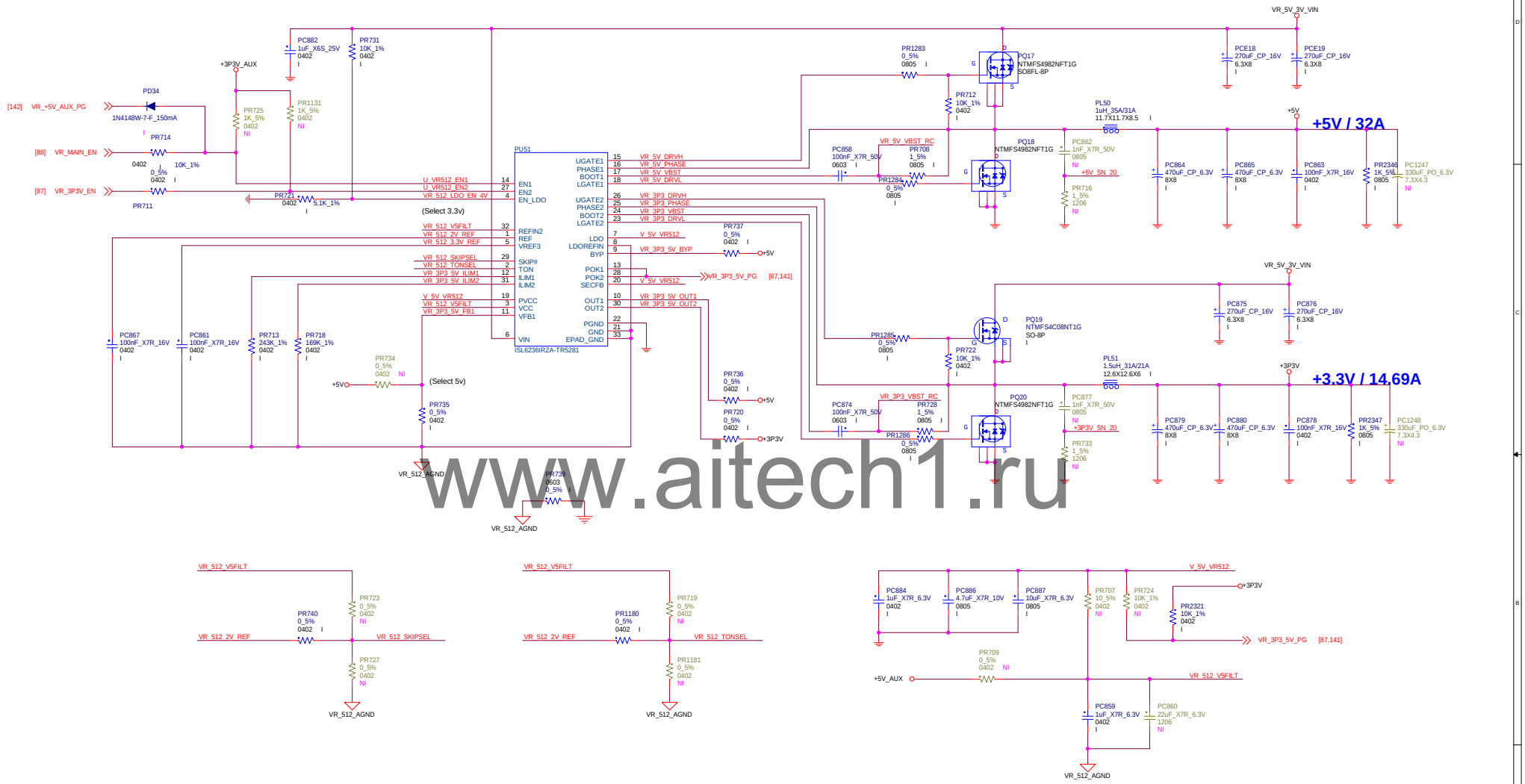
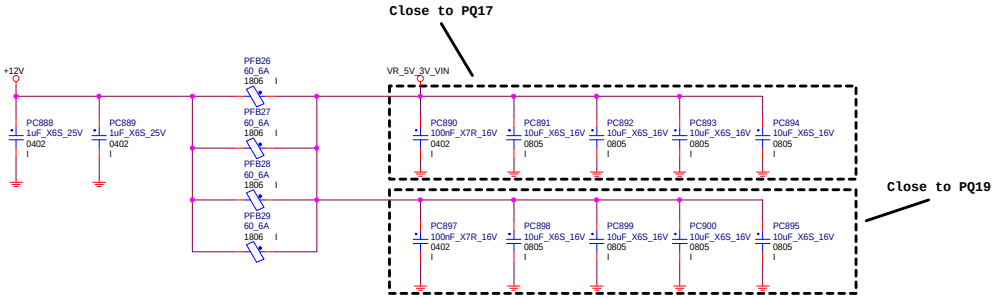
TITLE VR. 1P0V_AUX_PCH CONTROLLER		
DWG NO. MATIRA 3	REV. A00	
DATE Tuesday, June 13, 2017	SHEET 140 of 147	

COMPRESSED IMAGE

+3V / +5V





TITLE	VR_5V , 3.3V
DWG NO.	MATIRA 3
REV.	A00
DATE	Tuesday, June 13, 2017
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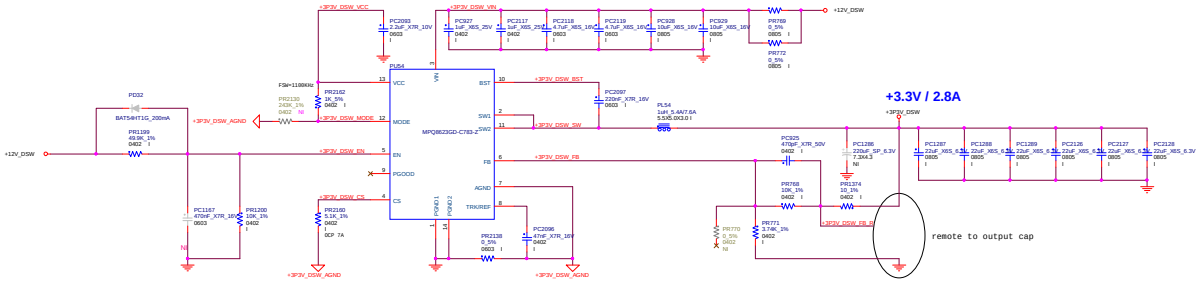
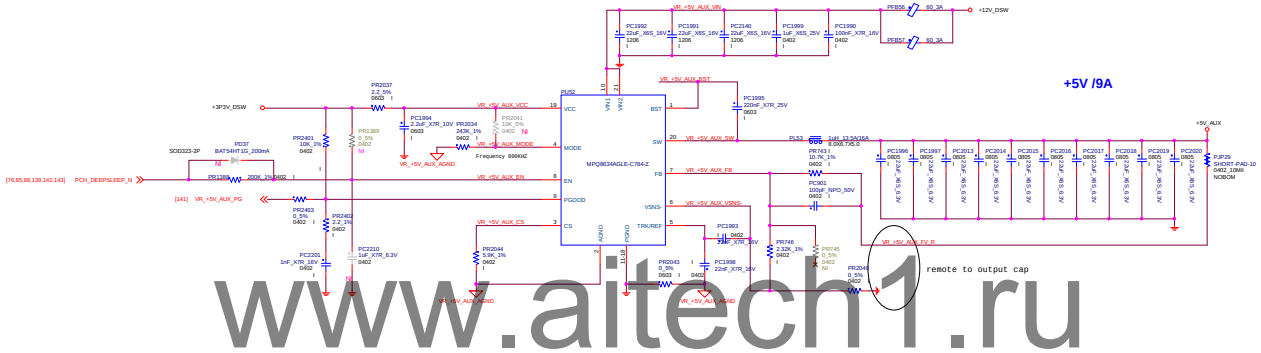
+3P3V_DSW

Modify 2/4 , VR change by ARD request to follow 14G PIG



+5V_AUX



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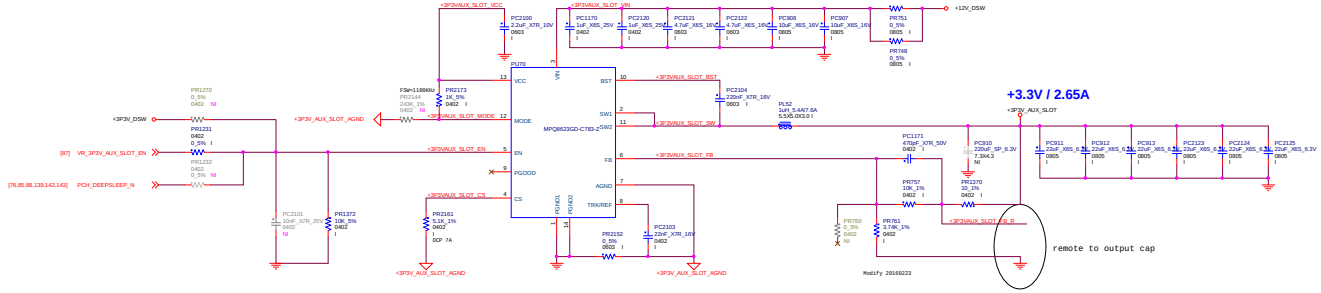
+3P3V_AUX_SLOT



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TITLE:	VR_+5V+3V_STDBY_CONTROLLER
DWG NO.	MATRA 3
REV	ADD
DATE:	Tuesday, June 13, 2017
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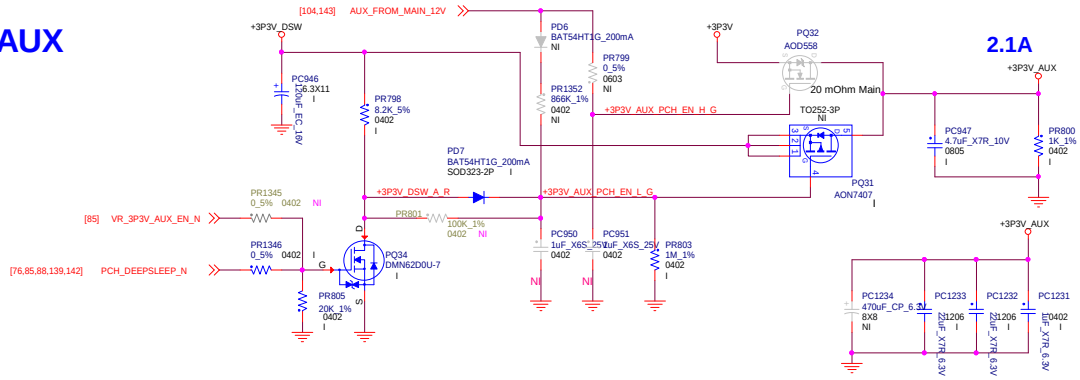
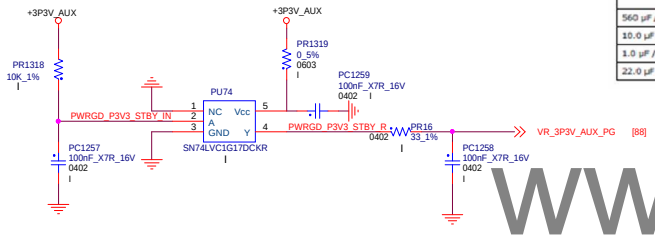
+3P3V_AUX

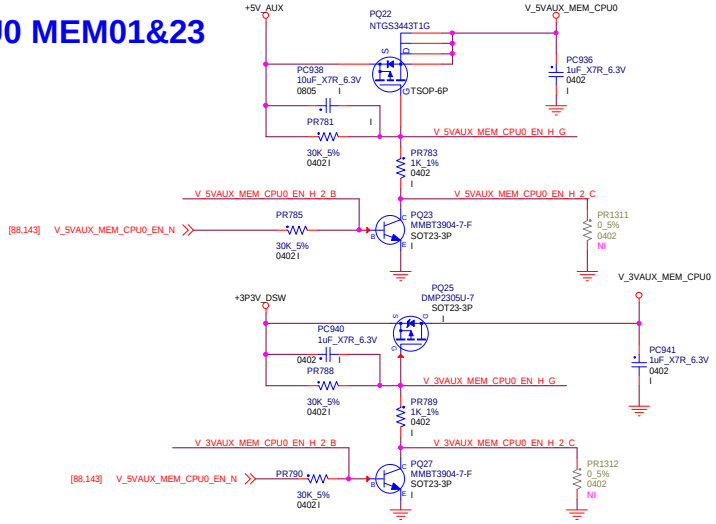


P3V3_AUX VR Decoupling Caps based on Neon City RB

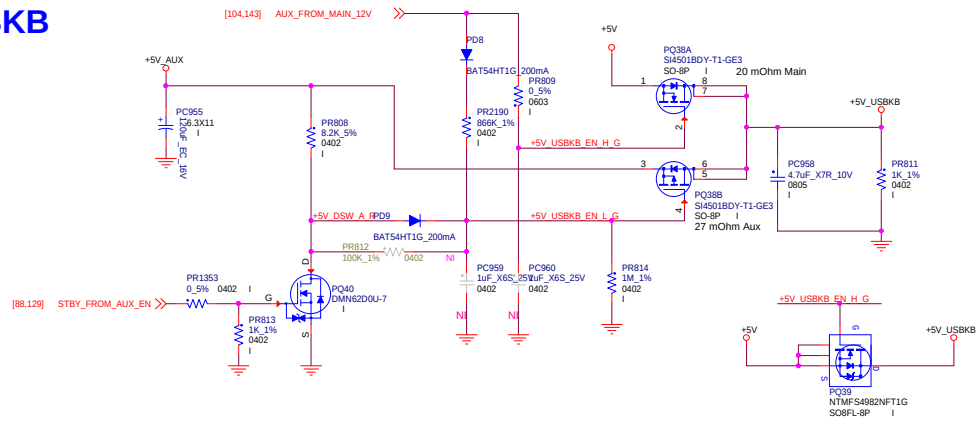
Cap Value	Min Quantity per VR	Notes
560 µF / 6.3V / 20% / Alum	1	Bulk, place close to VR output inductor
10.0 µF / 4.0V / 20% / X6S / 0603	6	
1.0 µF / 6.3V / 10% / X6S / 0402	3	
22.0 µF / 4.0V / 20% / X6S / 0805	2	Place close to VR output inductor



CPU0 MEM01&23



+5V_USBKB



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TITLE	VR. 5V_STBY,3.3_AUX		
DWG NO.	MATIRA 3	REV.	A00
DATE	Tuesday, June 13, 2017	SHEET	143 of 147

COMPRESSED IMAGE

+P2V5_CPU0 (Empty)

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TITLE	LOADSWITCH, +P2V5_CPU0 (EMPTY)	
DWG NO. MATIRA 3	REV. A00	
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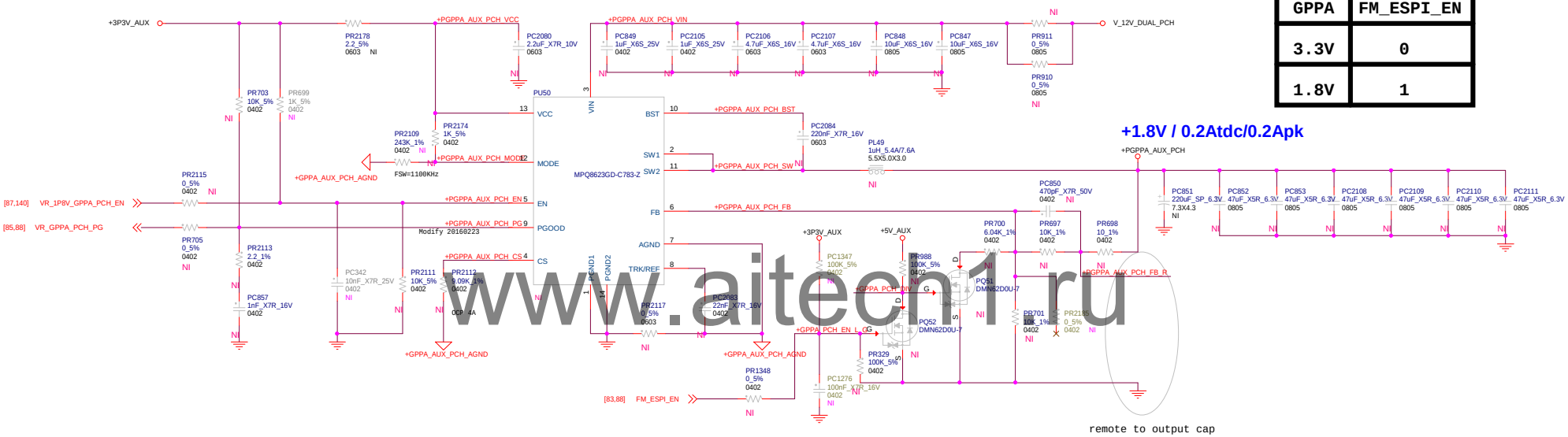
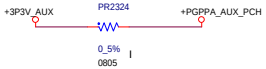
COMPRESSED IMAGE

PGPPA_PCH_AUX VR Decoupling Caps based on Neon City RB

Cap Value	Min Quantity per VR	Notes
220 µF / 6.3V / 20% / OSCON	1	bulk, place close to VR output inductor
22.0 µF / 6.3V / 20% / X6S / 0805	2	place close to VR output inductor (bottom layer)

GPPA	FM_ESPI_EN
3.3V	0
1.8V	1





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TITLE	VR, PGPPA_AUX_PCH		
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CONFIDENTIAL IMAGE

X00 modify color X01 modify color X02 modify color

X00 to X01 Changelist

20160908_1000 EE

P076:Add PCH DRAM_RESET# PU RS415 follow CRB0.79

P077:Add CPU_ERR2_N to PCH follow M5&7

P079,P087: Add PCH_TCM_DISABLE_N,add RS416

P106:Update reference QO45B to QO19B

P107:Add RF470,RF471 for TCM reset

20160912_1900 EE

Update PCH PN

P108:Update BIOS Lable PN

20160913 DC

P139: Remove NO_DEEP1 jumper from across PQ41.
Place it between PCH_DEEPSLEEP_N and +3P3V_DSW.
Change PR938 to 20K.
Add PR2360
P143:chang PR805 to 20K.

P142:PR2179 unstuff
ADD PR2401,PR2402,PR2403,PC2201
P141:Add PD34

P129:PC2142,PC2175 link datebase part
P131:PC2147,PC2148 link datebase part

20160914_1400 EE

P076:Modify RS5 from 0 ohm to 1.2k ohm for Non-deepsleep mode

20160919_1900 EE

Modify Title Block

20160920_1100 EE

P084:Modify RS111 from NI to I,RS112 from I to NI

P085:Add RST_I2C_PCA9546_N

P085,87,88,105,106:Modify FAN control base on EE Tracker

P069:Dummy SLOT2_CPU0_LATCH1
Modify SLOT2 from Blue to Black

P070:Dummy SLOT4_CPU0_LATCH1
Modify SLOT4 from Blue to Black

20160921_1000 EE

P088:Add PCH_SPKR Pin C5

P092:Del CA104,PCH_SPKR

P108:Modify BUZZER schematic follow M7

P085:Move SLP_S3# from Pin F8 to C11
Del PCH_PWRBTN_N for Pin D5,
and change RO29 from 0 ohm to 1k

20160921_1600 EE

P066:Modify Clock buffer circuit for LPC TPM

P107:Add circuit for LPC TPM

20160921_1700 EE

P092:Add CA104 del CA105

P108:Add PA1

20160921_1700 EE

P006:Modify sequence block

P078,P066:Modify sub-system

20161013 DC

P141:Change PR714 from 33 ohms to 10 kohms

20161017_1700 EE

Change All SATA/USB3.0/PCIe/DMI net name

P77:Swap USB3.0 port8 TX/RX signals to fix X00 issue.

P19:Populated RH53.

P109:Change RH261 PU to +3D3V_DSW to follow CRB.(Leakage issue)

P83:Change RS138 PU to +3P3V_AUX.(Leakage issue)

P89:Populated RL3.(M7)

P85:Dummy RO434/RO482/RO483.(M7)

P92:Dummy RA30 and populate RA29.(M7)

P084:Del PW_CMOS_SERVICE;add PSWD,CMOS_CLR,SERVICE_MODE.(M7)

P085:Modify RO487,RO489,RO491,RO493 from 0 ohm to 4.7K ohm.(M7)

P084:Modify RS111, RS110, RS114, RS79, RS80 to 1K ohm.(M7)

20161018_1500 EE

P019:Change RH160/RH163 to 75ohm. (follow CRB)

P105/87/88:Change FAN control circuit from 2303 to 2305 and add CPLDfan control for FAN_REAR0/FAN_REAR1.
P106:Add FAN_REAR0/FAN_REAR1.

20161024 DC

P140:Change PR291 from 6.81K ohms to 3.57 kohms

P140:unstuff +1P8V_AUX_PCH VR

20161025_1500 EE

Change USB Power Switch from DIODES_AP22802AW5-7 to RICHTEK_RT9742CGJ5F

P066:Change Clock buffer from DFN-8P to TSSOP-8P

P108:Modify CA117 to TMK107B7105KA-T.(M7)

20161026_0900 EE

P079:Change TPM_CS# to SPI_CS2#

P092:Modify RA2 from 22 to 33

20161026_1600 EE

P105:Modify RO509-RO518 from NI to I
P106:Modify QO45B to QO20B,QO46B to QO15B
P107,P066:Modify TPM_RST&TCM_RST(M7)
P111:Modify PCB info
Modify PCH PN
P082:Modify PCH_Heatsink PN
P075:Modify MINISAS_SCREW PN
Modify CPLD PN

20161027_1100 EE

P105:Modify UO17 to UO16 and net name

20161027 DC

P128£ºPR2215 change from 294K to 267k 1%
PR2240 change from 39k to 24k 1%
P129£ºadd 100nF PC2202 paralle to PC2142
add 100nF PC2203 paralle to PC2175

P130£ºPR2258 change from 294K to 267k 1%
PR2281 change from 39k to 24k 1%
PR2268 chagne from 71.5k to 44.2k 1%

P131£ºadd 100nF PC2204 paralle to PC2147
add 100nF PC2205 paralle to PC2148

20161028_1400 EE

Combine DC schematic

20161028_1430 EE

P105:Add DIMM Thermal Senor UO1 circuit

20161028_1500 EE

P105:Modify Thermal Control UO16 circuit base on EE Tracker

20161028_1800 EE

Modify PCH info

20161031 DC

P142.:change PR2160 From 7.5K to 5.1K
change PR 2161 from 7.5K to 5.1K

20161031_0900 EE

Modify CPLD info

P089:Modify CL8 from 22pF to 27pF base on Vendor's Report

20161031_1500 EE

P108:Modify BEEP CCL from N to Y

P141:Modify PD34 CCL from N to Y

20161102 DC

P128:Stuff PR128,chang PR128 from 100 ohm to150 ohm
P130£ºchang PR167 from 100 ohm to 150 ohm
P113: stuff PR2331,PR2332,PR2333,PR2335

20161107_0900 EE

P025:Update CPU0_BSDC footprint form NPTH to PTH

P106:Swap FAN_SYS0 and FAN_SYS2 reference

P103:Change DMN65D8LDW-7 to DMN62D0UDW-7

20161107_1500 EE

P025:Connect CPU0_BSDC to PTH

20161107_1700 EE

P089:Change QL6 from AO4453 to SI4835DDY-T1-GE3

20161108_1700 EE

P076:Change CS1&CS2 from 12pF to 15pF base on Vendor's Report

P106:Add FAN_CPU 7Pin co-lay with 5Pin circuit

20161108_1700 DC

P143:Change PQ31 to AON7407 from SISS27DN-T1-GE3

20161110_1000 DC

P136:Dummy PR237&PR220

20161110_1000 EE

P106:Swap FAN_SYS0 and FAN_SYS2 reference

P111:Modify Insertion Loss PCB GND
differnt from MB GND for Layout

P085:Modify EC from MEC5105K-D1-TN to MEC5105K-D2-TN
P105:Add THERM_ODD header and connect to EC.B10&A11

20161111_1400 EE

P104:Add RS417 for Frontpanel Cable detect Pull-up

P105:Modify Thermal_ODD Header from 2Pin to 4Pin,
connector cable detect to Page79 PCH GPP_G20

P106:Modify RO315&RO82&RO92 Pull-up from +3P3V_AUX to +3P3V
Modify RO121 from NI to I
Add FAN_CPU TACH +12V to +3P3V Level shift

20161111_1400 EE

P106:Modify FAN_CPU TACH +12V to +3P3V Level shift

20161112_1600 EE

P084:Add Air Shroud Dectection Switch follow M5

20161115_1100 EE

P105:Combine Thermal HDD and ODD Header to one 2x6 Header
base on SE's suggestion
P075:Modify MiniSAS CONN footprint to Vertical CONN footprint

20161115_1700 EE

P077:Add RS282 THUNDERBOLT cable detect Pull up

20161116_1130 EE

P084:Delete Air Shroud Dectection Switch follow DM'S comment

20161117_1330 EE

P098:Delete Redriver and 0ohm co-lay circuit

20161122_1000 EE

P075:Update MINISAS CONN PN
P092:Dummy RA27 and QA4,Stuff RA30 and add RA65
Modify net name AUD_FP_SLEEVE_GND to AUD_FP_SR_GND
(For Cold boot can't detect NOKIA headset issue)
P106:Dummy RO523,stuff RO526
P105:Update Thermal Header PN

20161123_0900 DC

P141:Change PR718 from 86.6K to 169K
chang PR713 fome 169K to243K

20161123_0900 EE

P075:Add RX125&126
P105:Modify THERMAL_HDD_ODD to THERM_HDD

20161123_1100 EE

P075:Update MINISAS PN
Update PCH PN

20161123_1400 EE

P075:Delete RX125&RX126
Update USB Power Switch Enable Pin from +3P3V_AUX
to +5V_USBKB,except power share Port6

20161123_1600 EE

P092:Dummy RA30,stuff RA29

20161124_1430 EE

P023:Swap PE_HP_SDA wtih PE_HP_SCL

P105:Update Therm_HDD CONN PN

20161124_1700 EE

P079:Add RS418 Pull up for TBT_SCI_EVENT(Follow M7)

Update PCB info for BOM

20161126_1000 EE

Update Parts Side properties

P075:Modify MINISAS CONN screw from 1PS-20050-TLEQ to
TPS-20050-1TLEQ(Follow M7)

20161126_1100 EE

Update Parts Side properties

20161126_1500 EE

P105:Modify UO1&QO46&QO47 CCL from N to Y
P025:Modify CPU0_BSDC CCL from N to Y
P112:Modify PU1 CCL from N to Y

X01 to X02 Changelist

20161228_0900 EE

P077:Dummy RS10,RS14,RS398 for function not use.

P076:Follow CRB0.9 add TP134

P075:Dummy UX2&UX3,stuff RX52&RX53 to support LSI Card

P093:Change DA11&DA9 from PROTO to NI,
Change DA8&DA6 from PROTO to I

P084:Change VROC_KEY from MOLEX to PINREX due to cost

P079:Added PCIE Slot Present Detect(Follow M7)

20170102_1700 EE

P064:Modify RH440&RH444&RH448 from 22k to 499
RH443&RH449&RH445 from 75 to 200(Follow M7)
P088:Modify DO3 from I to PROTO(Follow M7)

20170106 DC

P104:POWER1 change to 4122112419-0211 from 4122112419-0212

P138:Dumy PCE36£¬PCE37
change PC221,PC222,PC232,PC233 to 47uf from 22uf
short PC225,PC235
change PR203£¬PR212 to 5.1K ohm from 3.9K ohm

20170106_1630 EE

P104:Add RS419 for USB_OC1 due to EMD test MB without FIO

20170112_1130 EE

P106:Modify RO497 PU from +3P3V_AUX to +3P3V

Due to cost up,follow DELL feedback change material as below

P084:Modify SERVICE_MODE from I to Proto

P093:Modify AUDIO from GOLD 25uf to Gold Flash

P105:Modify UO16 from I to NI

P108:Modify PWR_REMOTE from Gold Flash to Tin

P106:FAN_SYS1,FAN_REAR1,FAN_SYS2,FAN_SYS0,FAN_REAR0 from Gold Flash to Tin

P106:FAN5_CPU,FAN_HDD from Gold Flash to Tin

P084:TBT from Gold Flash to Tin

P097:USB2_FLEX from Gold Flash to Tin

P075:MINISAS_HD change to 2 x LY50363-N6S0-0H (FLEX0 & FLEX1 same as M5)
remove MINISAS_SCREW1 / MINISAS_SCREW2 / MINISAS_SCREW3

20170112_1600 EE

Follow DELL Terry's request20170111
P102:Modify SATA Port Mapping follow M5 due to SIT SATA Port Mapping issue

20170113_1100 EE

P084:Modify TBT symbol

P106:Modify FAN5_CPU&FAN_HDD symbol

20170117_1900 EE

Modify below items base on EE Tracker DELL_20170116

P084:Modify CMOS_CLR name to CMOS

P105:Dummy CO266&RO508&RO389&RO370&RO369

P087:Add GPI_INTRUDER_CABLE_DET_N to CPLD Pin.p13

20170118_1900 EE

P066:Modify TCM sub system to CHINA TPM

P078:Modify RS255&RS256 from MP to NI

P088:Modify DO3&RO195&RO201&RO205&RO203&CO85&CO84 from PROTO to I

20170118 DC

P128:PR2215 change from 267K to 249K

P130:PR2258 change from 267K to 249K

20170119_1100 EE

P111:Update PCB PN

20170119_1100 EE

P111:Modify PCB info

P093:Modify AUDIO back to GOLD 25uf(due to mold is too old)

20170216_0900 EE

P105:Modify HDD TEMP circuit follow M5

P079:Add HDD_TEMP_DET2# GPIO

20170220_0430 EE

P078:Add EC_LPC_SMI_N pull up RS420 follow M7

20170221_1630 EE

P093:Modify Audio CONN reference name to AUDIO

20170223_1630 EE

P071:Stuff RK30 follow M5 for PCI LAN wake function

P072:Stuff RK9 follow M5 for PCI LAN wake function

20170227_1500 EE

P087&P88:Modify CPLD PN from LCMXO3LF-2100C-5BG256C
to LCMXO3LF-2100C-5BG256C7U
and need add LCMXO3LF-2100C-5BG256C as 2nd source

20170228_1500 EE

P105:Modify Thermal Diode QO41&qo42 footprint base on EMD request

P108:Add BIOS Label Footprint and modify reference from LBL1 to BIOS_LABEL

P084:Modify Board Revision ID to X02(010)

20170304_1100 EE

P094&95&97&99:Modify OC Pull up

20170304_1100 EE

P076:Modify RS207 from 1M to 150K and pull up from +3P3V_DSW to +3P3V_AUX

201700306 DC

P139:PR2360 change from 100 oHM to 1K

20170307_1500 EE

P025:Dummy RH48&RH59,stuff RH73 to enable TXT function

20170307 DC

P025:P139:Add a dumy PD36

20170311_1600 EE

P083:Modify RS265 from I to PROTO(Follow M7)

P107:Modify SPI_1 from W25Q256FVFIQ to W25Q256JVFIQ,due to cost as DELL request

20170311_1600 DC

P142:change PR1388 from 0 ohm to 20k ohm.
change PR2179 (10k ohm) to PC2210 (1uf)
add PD37

20170313_1500 DC

P142:dumy PD37&PC2210
Change PR1388 from 20K ohm to 200K ohm

20170316_0900 EE

P097:USB2_FLEX back to Gold Flash

P088:Add PCH_SUSACK_N&PCH_SUSWARN_N for VDDQ pulse issue when S0-->Deep S5

20170316_0900 EE

P075:Modify FLEX1_P0 to PCIE0 and FLEX1_P1 to PCIE1

P088:Add RO529&RO530 for PCH SUSWARN&SUSACK

20170317_1000 EE

P085:Modify RO385&RO386&RO387 from PROTO to I
Dummy RH289&RH470(Follow M7)

P077:Add RS421 for SMI debug
P078:Add RS422 for SMI debug
P077:Move FM_TBT_SCI_EVENT from GPP_H17 to GPP_E1 to support SMI Event

P077:Move SLOT4_B12_EVENT from GPP_D22 to GPP_E2 to support SMI Event

P079:Add RS423&RS424&RS425(Follow M7)

20170320_1700 EE

P078:Modify RS23 from 10K to 1K(Follow M7)

P078:Delete RS422,RS421,reserve TP135

20170323_1000 EE

P108:Delete BIOS Label footprint follow EE Tracker

20170324_1000 EE

P106:Dummy FAN_REAR0&FAN_REAR1 follow Thermal test result

20170325_1000 EE

P083:Change RS136 from NI to MP follow M7

20170327_1000 EE

P085:Change RO124 from NI to I to support PS2 KB/MS wake

P108:Change BIOS_LABEL from I to NI follow DELL request

20170330_1900 EE

Update RH443&RH449&RH455&RX52&RX53&RH440&RH444&RH448 from TOP to BOTTOM
Update RO529 from BOTTOM to TOP

20170331_1000 EE

Update RH440&RH444&RH448 to BOTTOM

20170401_1000 EE

P108:Change BIOS_LABEL from NI to I follow BPM request

X02 to A00 Changelist

20170405 DC

P136:Change PU23,PU24 from MPQ8634AGLE-Z to MPQ8634AGLE-C784-Z

P140:Change PU26 from MPQ8634AGLE-Z to MPQ8634AGLE-C784-Z
Change PU49 from MPQ8623GD-Z to MPQ8623GD-C783-Z

P142:Change PU54,PU70 from MPQ8623GD-Z to MPQ8623GD-C783-Z
Change PU52 from MPQ8634AGLE-Z to MPQ8634AGLE-C784-Z

P145:Change PU50 from MPQ8623GD-Z to MPQ8623GD-C783-Z

20170505_1630 EE

P107:Change SPI_1 from DIP to SMD

P085:Change SPI_2 from DIP to SMD

P076:Change RS27 from I to NI

P111:Change PCB PN and Info

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COMPRESSED IMAGE

20170518_0930 EE

P109:Change RH290 from PROTO to I

20170523_1530 EE

Follow DELL Terry's suggestion add USB3.0 RX AC Cap and discharge resistor
P094:Delete RU59,RU60,RU67,RU68,add CU437,CU438,CU439,CU440,RU700,RU701,RU702,RU703
P095:Delete RU188,RU189,RU192,RU193,add CU431,CU432,CU433,CU434,RU704,RU705,RU706,RU707
P099:Delete RU681,RU682,RU683,RU684,add CU445,CU446,CU447,CU448,RU708,RU709,RU710,RU711

20170524_1500 EE

P094:Delete LU6,LU10
P095:Delete LU25,LU27
P099:Delete LU49,LU52

20170602_1100 EE

Base on DC comment
P028:Change CH22, CH23, CH24, CH25, CH26, CH27, CH32, CH33, CH34, CH35, CH36, CH37, CH38, CH39,
CH40, CH41, CH52, CH53, CH54, CH55, CH56 from 22uF_X6S_4V to 47uF_X6S_4V

20170606_1730 EE

Update some parts side properties

20170607_1030 EE

P104:Dummy RS419 for USB Hub(Self-power) wake issue

P111:Add Mylar to prevent Add-in Card bracket damage base on SE's request

20170609_1430 EE

P084:Update Revision ID:Change RS111 from NI to I and RS112 from I to NI

Update PCH PN

20170609_1430 EE

P111:Update Mylar and PCB PN

20170703_1500 EE

P107:Add @SPI_1 Lable and FW information
P085:Add @SPI_2 Lable and FW information
P087:Add @CPLD0 Lable and FW information

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TITLE: Changelist
SIZE:
DWG NO. MATRIX.3
REV: A00
SCALE:
DATE: Monday, July 03, 2017
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